

AMD KABINI EA/EG-40/50  
PX /UMA Schematics Document  
AMD FT3 APU  
AMD GPU SUN XT M2/64bit  
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EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A4

Document Number

**KABINI**

Rev

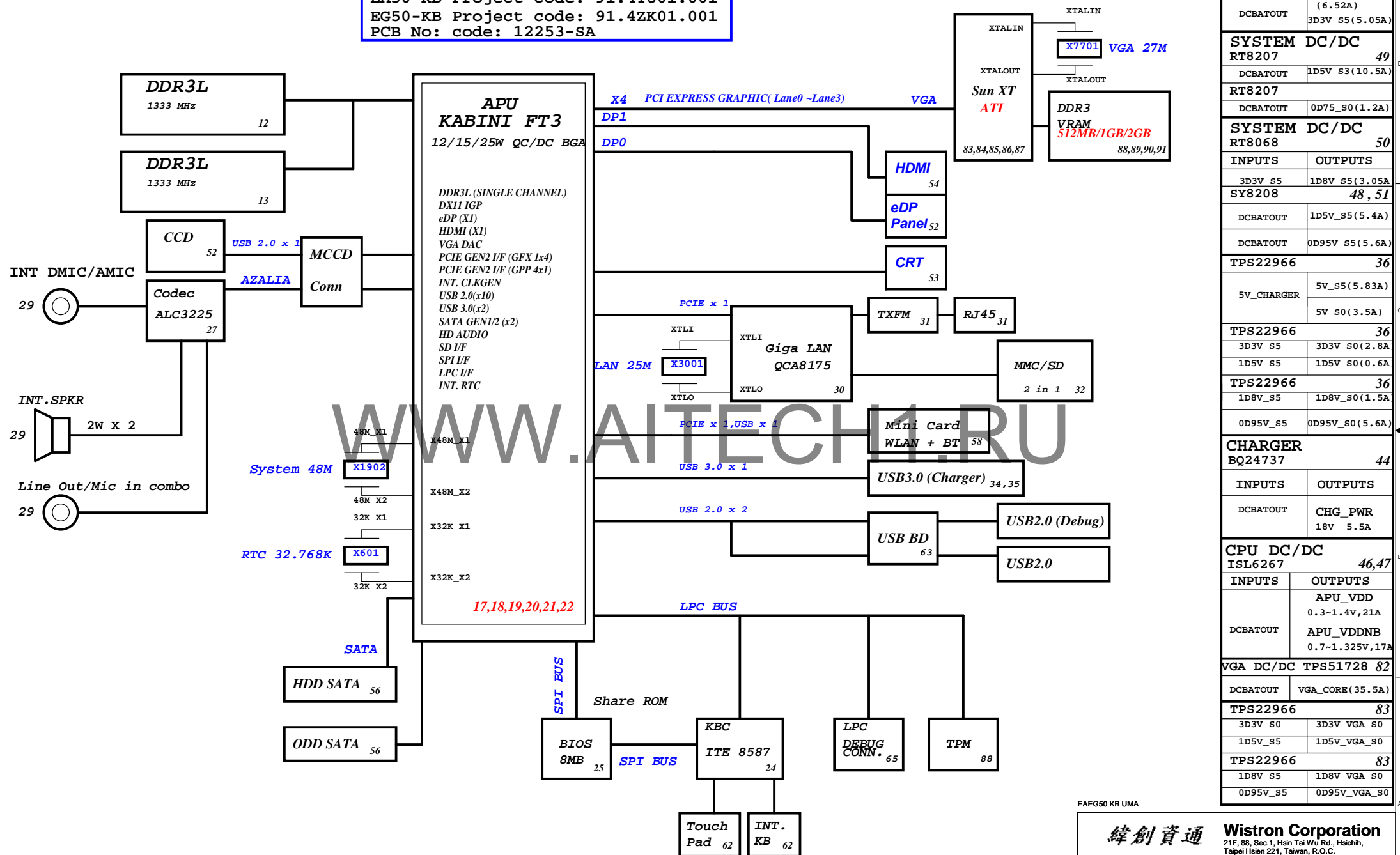
Date: Wednesday, October 24, 2012

Sheet 1 of 102



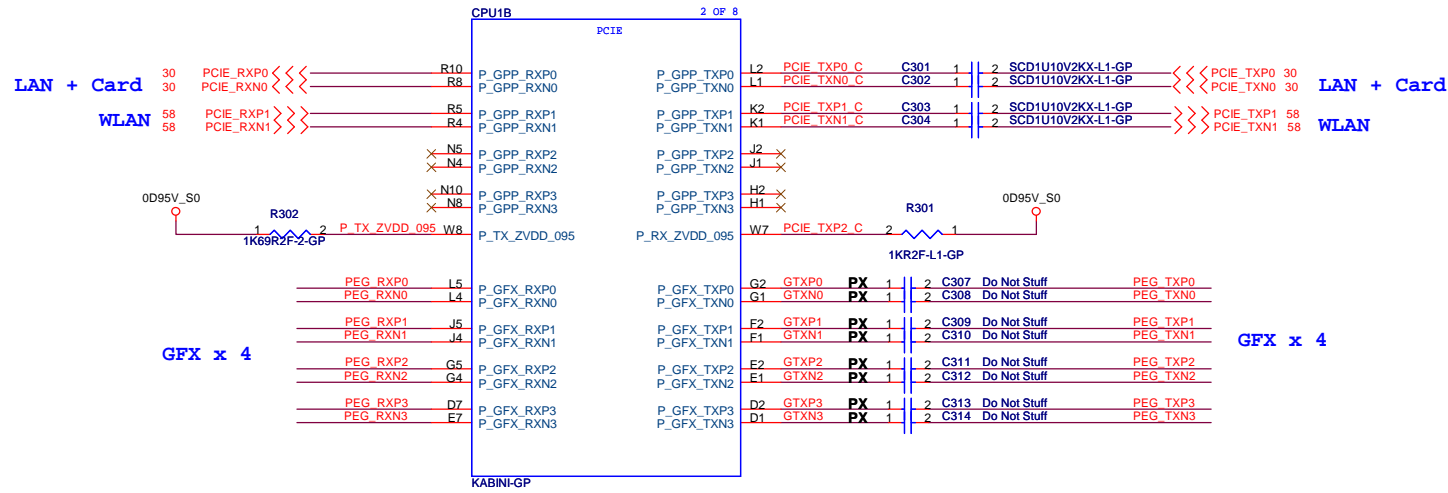
# AMD KABINI

EA40-KB Project code: 91.4ZF01.001  
PCB No: code: 12247-SA  
EA50-KB Project code: 91.4YU01.001  
EG50-KB Project code: 91.4ZK01.001  
PCB No: code: 12253-SA



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PCIE Table

0	LAN + Card
1	WLAN
2	NC
3	NC

71.KABIN.B0U IC CPU Kabini 4110 1.5GHz 15W4C FT3 ES2 BGA  
71.KABIN.C0U IC CPU Kabini 5110 2.0GHz 25W4C FT3 ES2 BGA

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Title CPU PCIE		
Size A3	Document Number KABINI	Rev
Date: Monday, February 04, 2013	Sheet 3 of 102	



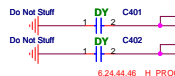
20120821 Follow Larne

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

20120820 Follow Larne

APU HDMI <

APU EDP <

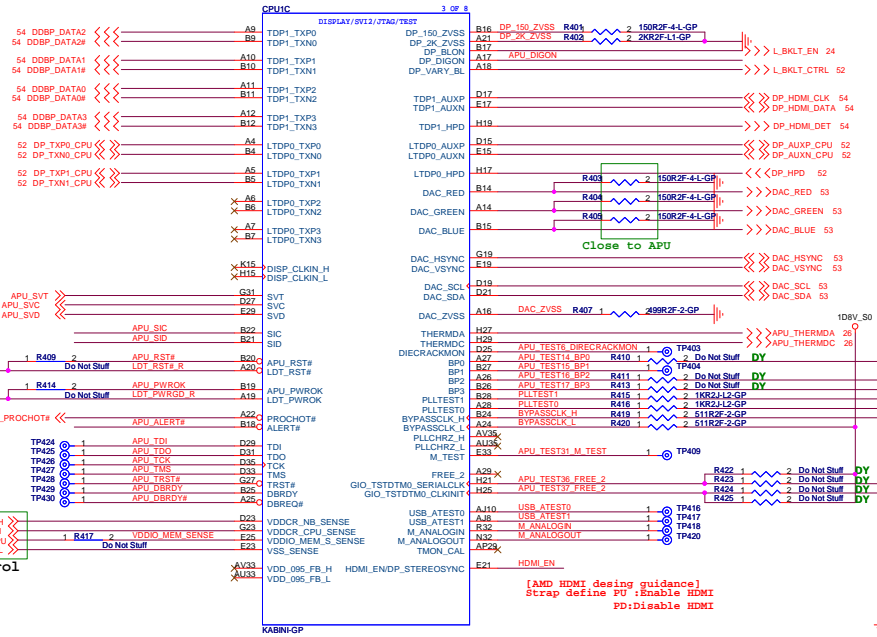


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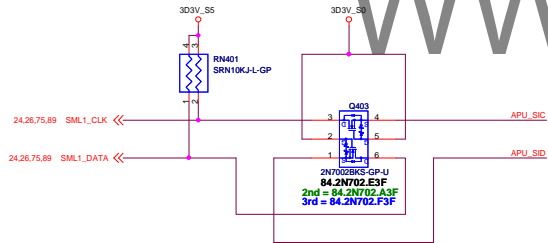
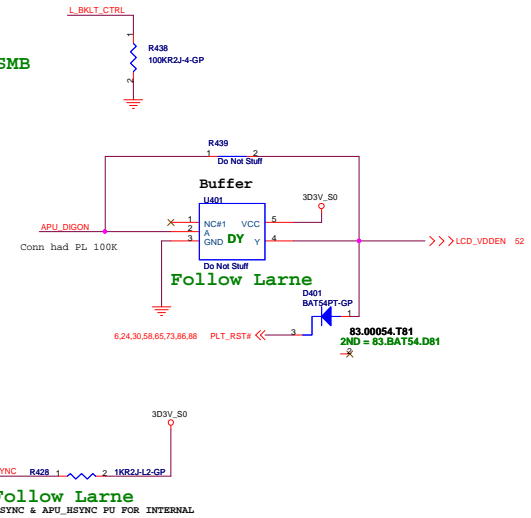
46 APU_VDDNB_RUN_FB_H
46 APU_VDD_RUN_FB_H
49 PWR_VDDQ_SENSE_APU
46 APU_VDD_RUN_FB_L

```

**APU core control**



- APU EDP
- APU HDMI SMB
- APU EDP
- APU CRT

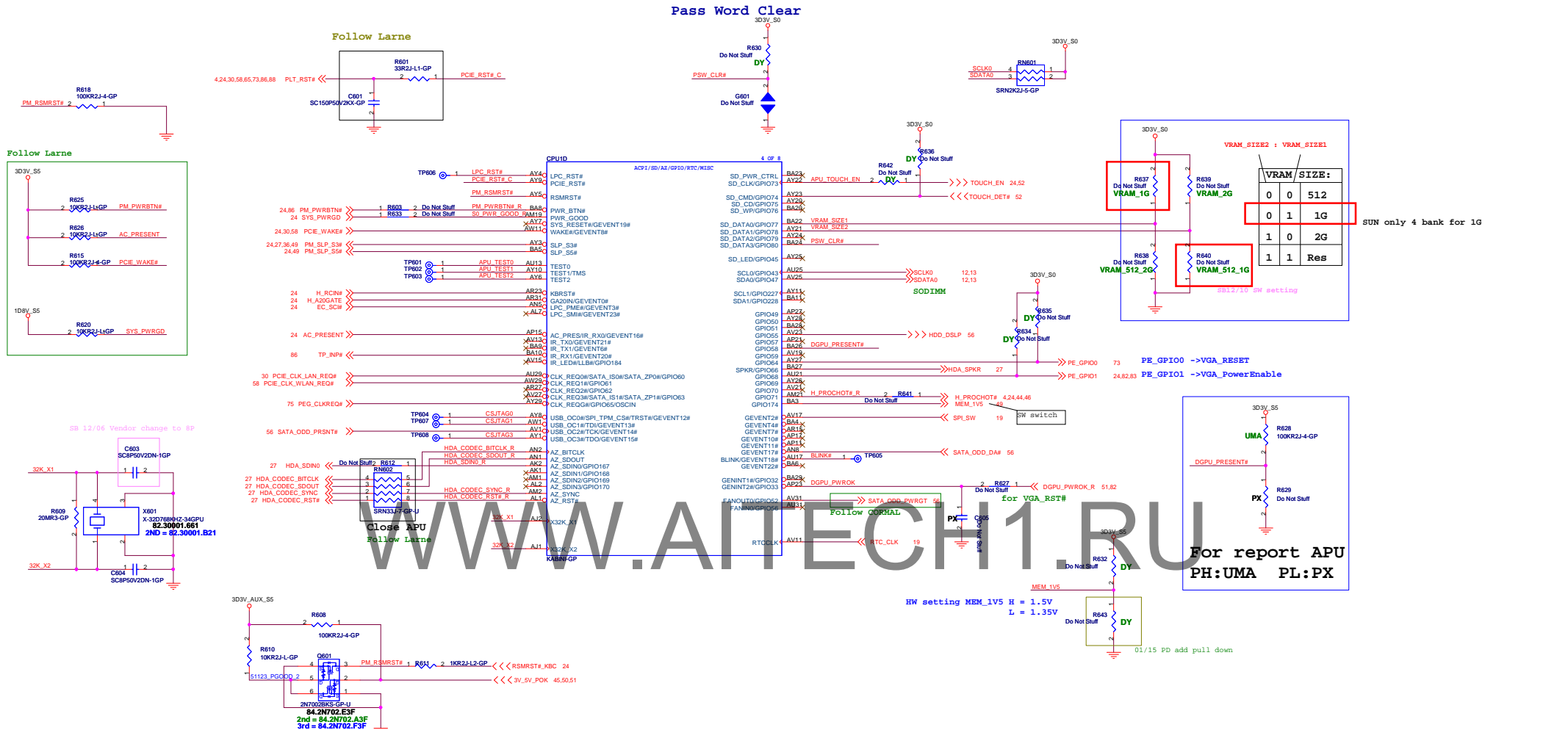


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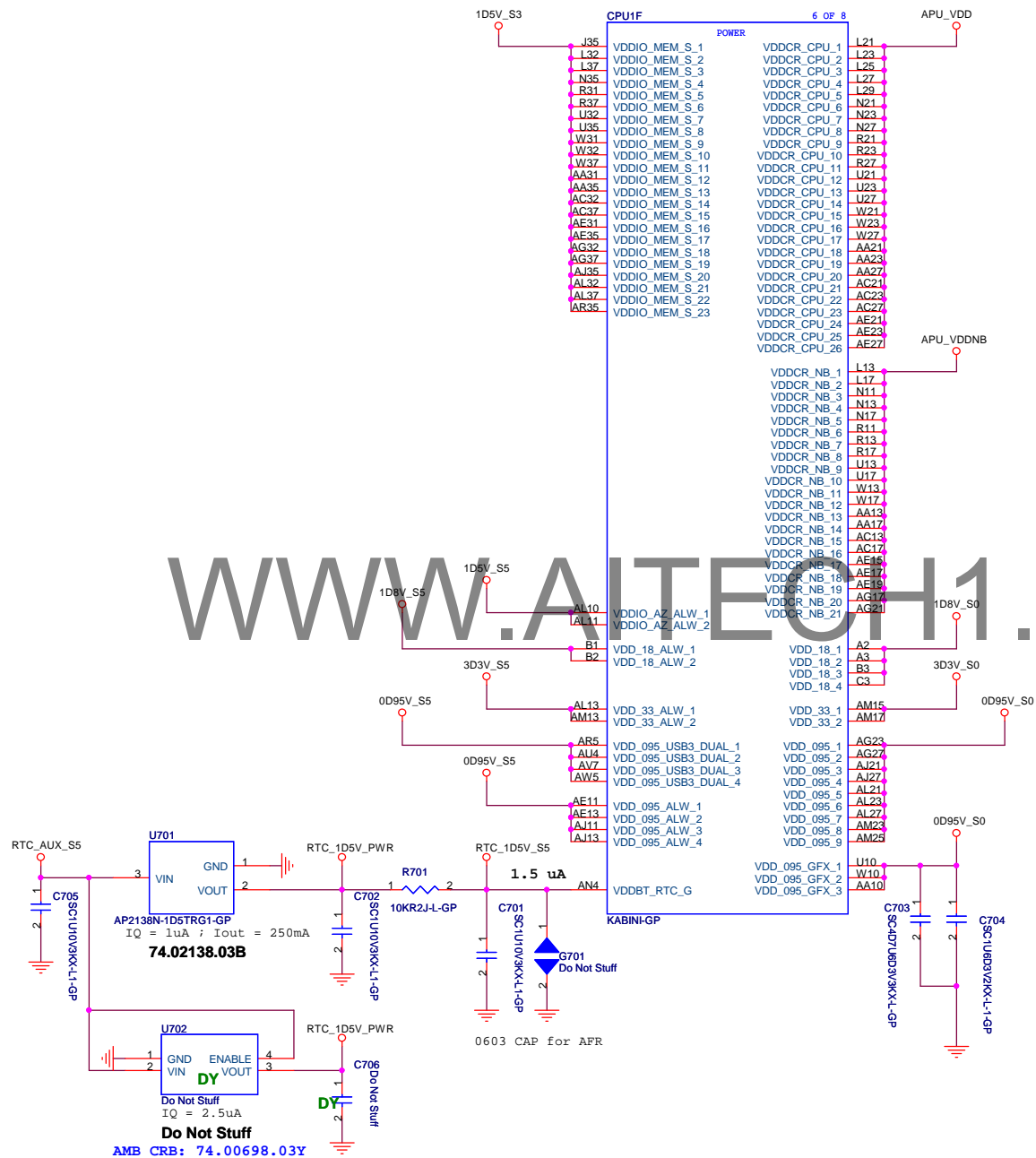












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Title		
CPU VCC CORE		
Size	Document Number	Rev
A3	KABINI	
Date:	Tuesday, January 15, 2013	
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Title

**CPU VCC GFXCORE**

Size  
A4

Document Number

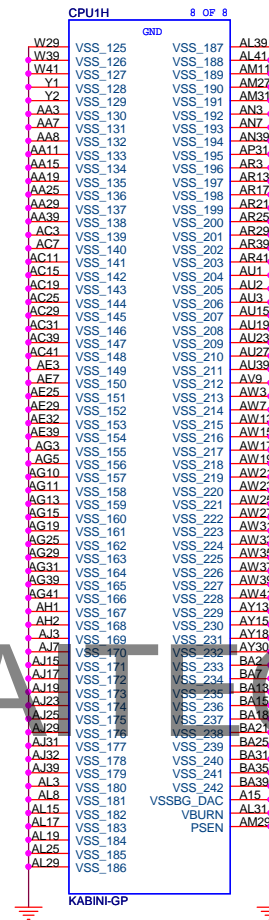
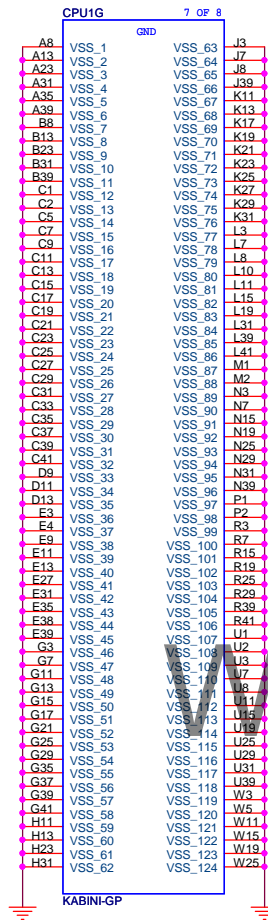
**KABINI**

Rev

Date: Friday, September 07, 2012

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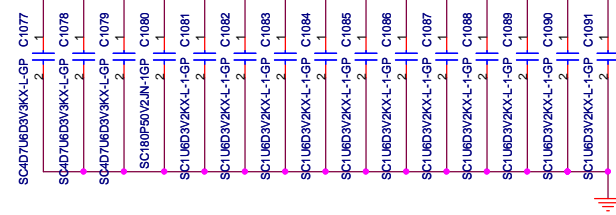
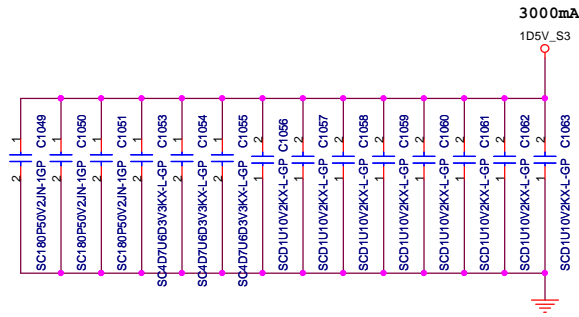
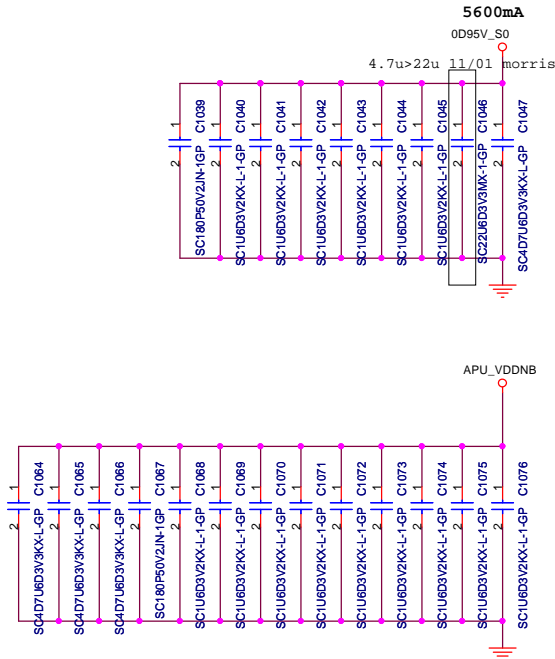
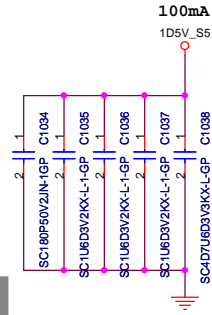
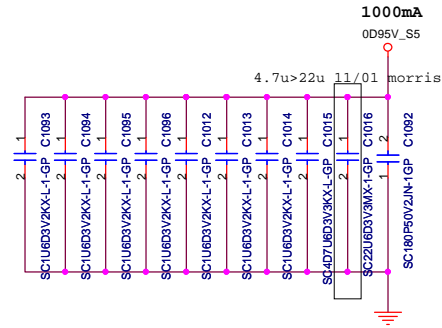
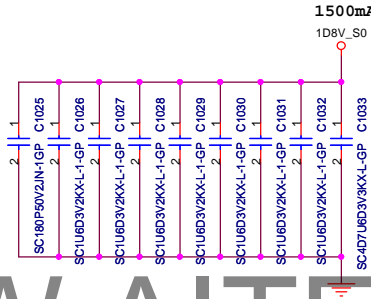
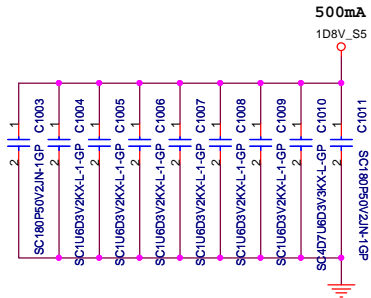
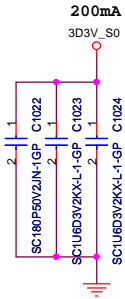
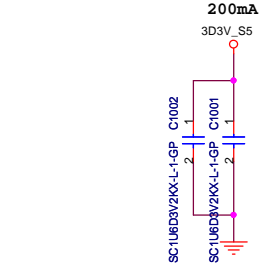




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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU VSS		
Size A3	Document Number KABINI	Rev
Date: Wednesday, November 28, 2012	Sheet 9 of	102





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Title		
CPU POWER CAP1		
Size	Document Number	Rev
A3	KABINI	
Date:	Tuesday, January 15, 2013	Sheet 10 of 102



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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CPU_POWER CAP2</b>			
Size A	Document Number		Rev
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Title

***DDR3 SODIMM 3***

Size  
A4

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Title **CPU\_EDP SIDEBAND/GPIO/DDI**

Size A4	Document Number <b>KABINI</b>	Rev
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Title

**CPU PCIE/USB**

Size  
A4

Document Number

**KABINI**

Rev

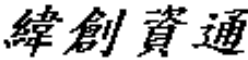
Date: Friday, September 07, 2012

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CPU DMI/FDI/PM		
Size A	Document Number <b>KABINI</b>	Rev
Date: Friday, September 07, 2012	Sheet 17 of	102



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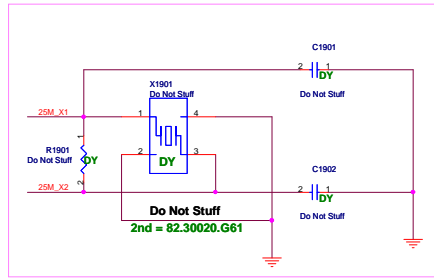
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Title <div>CPU_PCIE/SMBUS/CLK/CL/SPI</div>		
Size <div>A</div>	Document Number <div>KABINI</div>	Rev
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## SATA Table

0	HDD
1	ODD

SB 11/27 25M XTAL Reserved for AMD



VGA 73 PCIE\_CLK\_VGA  
73 PCIE\_CLK\_VGA  
30 PCIE\_CLK\_LAN  
30 PCIE\_CLK\_LAN  
58 PCIE\_CLK\_WLAN  
58 PCIE\_CLK\_WLAN

KBC 24.88 CLK\_PCL\_KBC  
DBB/TPM 65.88 CLK\_PCL\_LPC

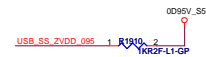
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## USB Table

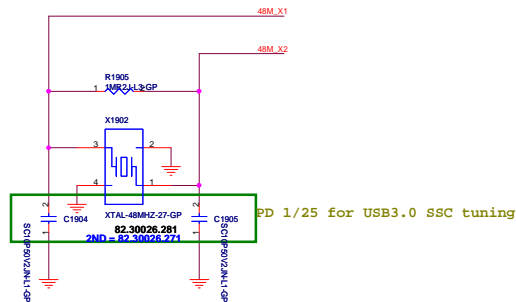
Pair	Device
0	USB2.0 Debug (DB Conn)
1	USB2.0 (DB Conn)
2	Touch Panel
3	
4	CCD (CCD Conn)
5	WLAN + BT (Mini PCI-E)
6	
7	
0/8	USB3.0 & USB 2.0 Charger (MB)
1/9	

## Xtal Table

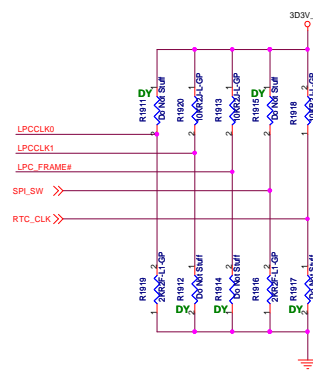
	System & USB	CLK
0	RTC	48M
1	SATA	32.768K
2	LAN	25M
3	VGA	25M
4		27M



SPI SHARE ROM



## SYSTEM STRAPPINGS



	LPC_CLK0	LPC_CLK1	LFRAME#	EXPCARD_PCIE_PWREN#	RTC_CLK
FULL	BOOT FAIL TIMER ENABLED	CLNGEN ENABLED	SPI ROM	1.0V SPI ROM (DEFAULT)	NORMAL POWR UP/RESET TIMING (DEFAULT)
HIGH		DEFAULT	DEFAULT		
FULL	BOOT FAIL TIMER DISABLED	CLNGEN DISABLED	LPC ROM	3.0V SPI ROM	FAST POWER UP/RESET TIMING FOR SIMULATION
LOW	DEFAULT				

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Title

**CPU GPIO/MISC**

Size  
A4

Document Number

**KABINI**

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Title

**CPU POWER1**

Size  
A4

Document Number

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Rev

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Title

**CPU RSVD**

Size  
A4

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Title

**CPU VSS**

Size  
A4

Document Number

**KABINI**

Rev

Date: Friday, September 07, 2012

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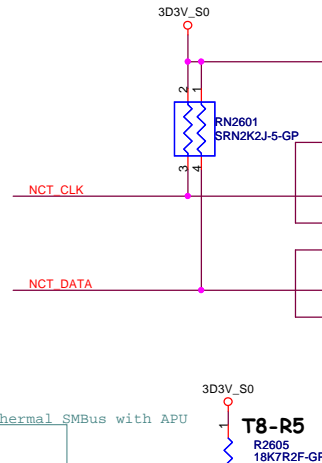
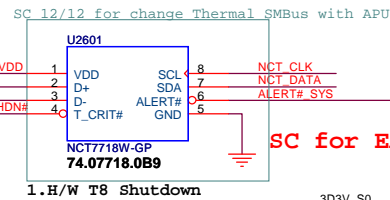
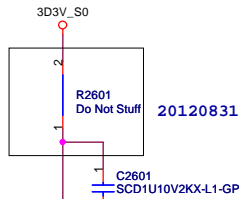
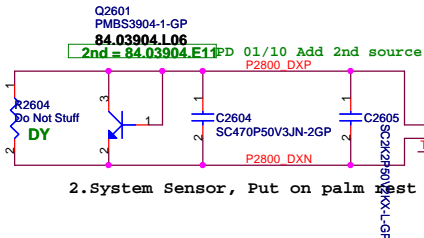




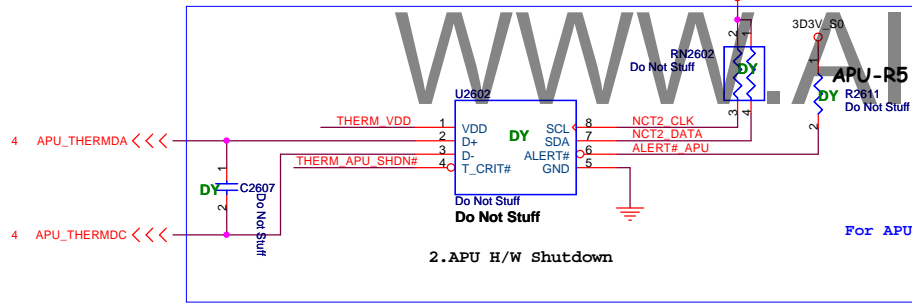
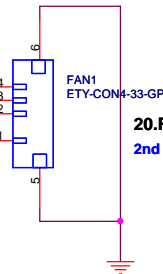
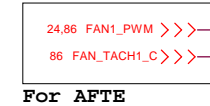
SSID = Thermal

## Thermal sensor NCT 7718W

Layout notice :  
Both DXN and DXP routing 10 mil  
trace width and 10 mil spacing.



SC EA50 DY RN2604 , mount RN2603



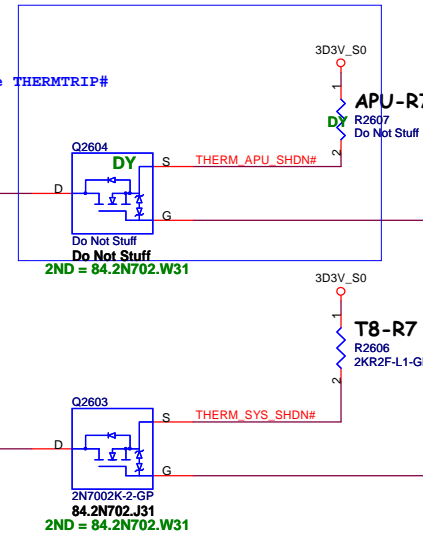
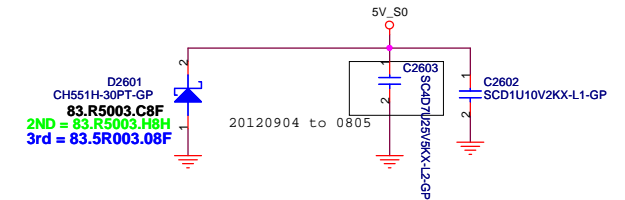
24,36 PURE\_HW\_SHUTDOWN# <<<

ALERT# /T CRIT#  
Pull-up Resistor

R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	87°C	97°C	107°C	117°C	
79°C	89°C	99°C	109°C	119°C	
81°C	91°C	101°C	111°C	121°C	
83°C	93°C	103°C	113°C	123°C	
85°C	95°C	105°C	115°C	125°C	

T\_CRIT temperature strapping point

T8=85 degree  
SYS=85 degree  
APU=125 degree



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Title Thermal 7718/Fan Controller P2793		
Size	Project Name KABINI	Rev SA
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Title

**AMP ALC1001**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

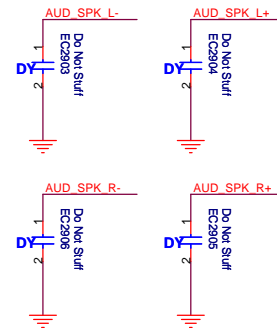
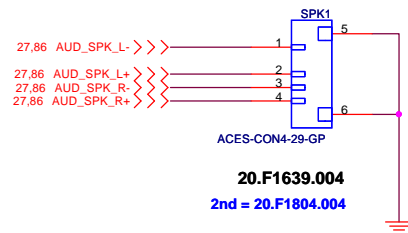
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SSID = AUDIO

## Speaker

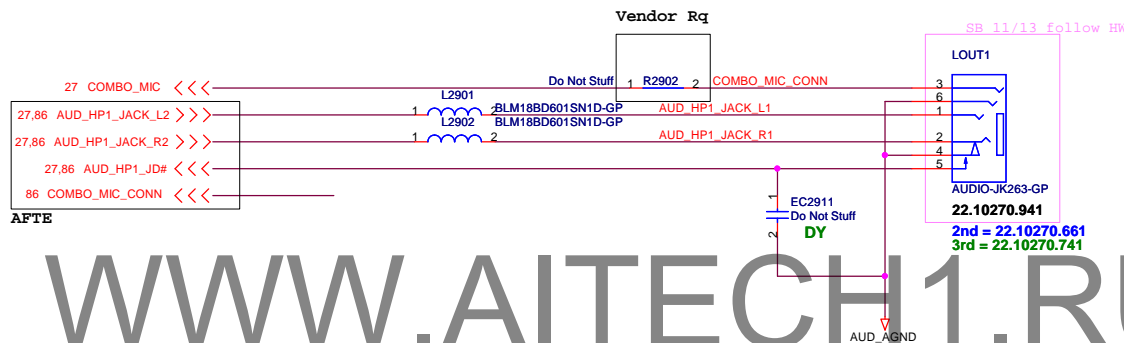
2W 4ohm X 2 speaker



Layout Note:

Trace width=40mil

## Combo Jack



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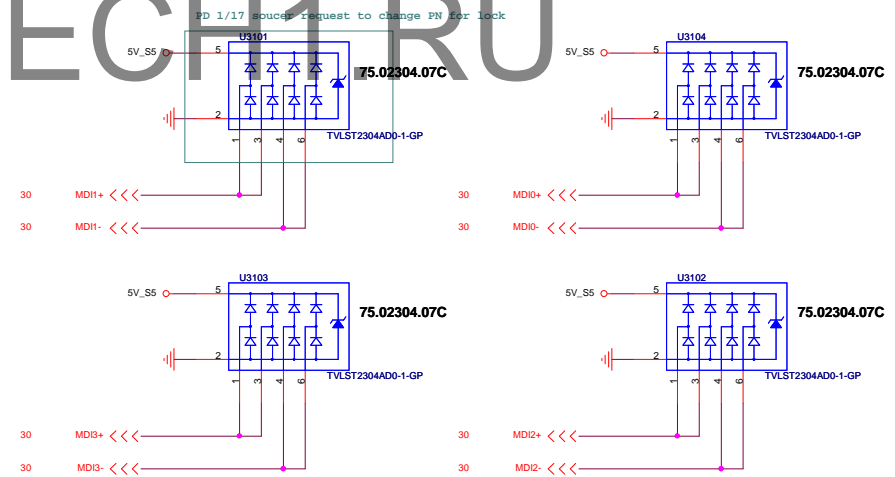
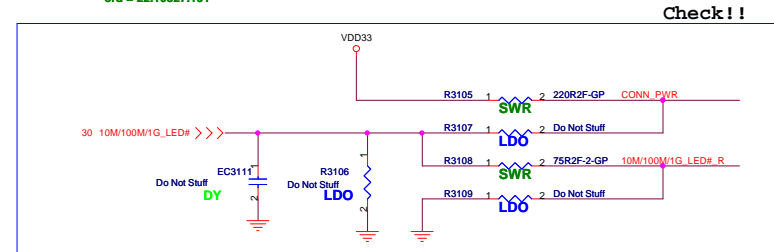
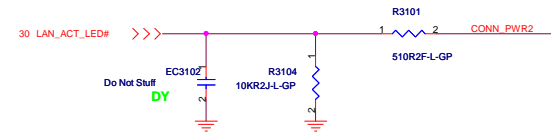
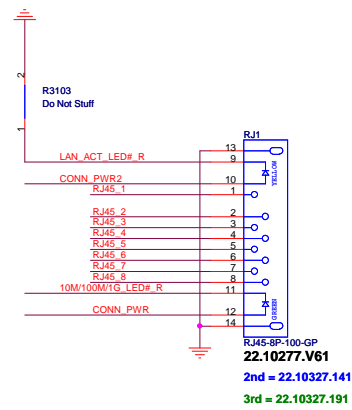
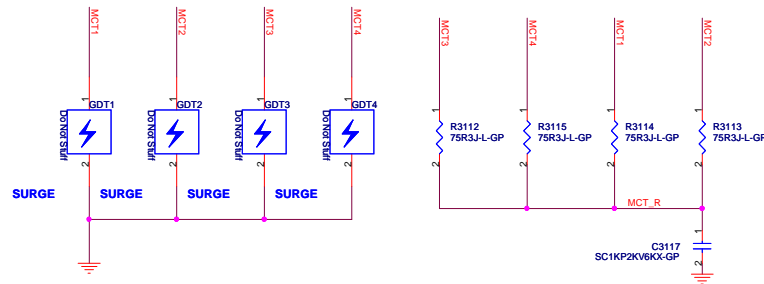
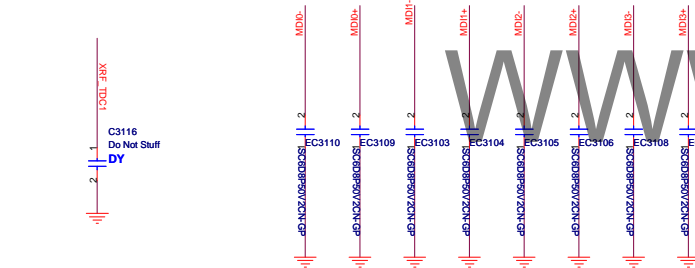
Title		Audio Jack	
Size	Project Name	KABINI	
Date:	Monday, February 04, 2013	Sheet	29 of 102
Rev	SA		







SSID = LAN



```

86 RJ45_1 >>>_____
86 RJ45_2 >>>_____
86 RJ45_3 >>>_____
86 RJ45_4 >>>_____
86 RJ45_5 >>>_____
86 RJ45_6 >>>_____
86 RJ45_7 >>>_____
86 RJ45_8 >>>_____

86 LAN_ACT_LED#R >>>_____
86 10M/100M1G_LED#R >>>_____
86 CONN_PWR >>>_____
86 CONN_PWR2 >>>_____

```

For AFTE



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Title

**Card Reader IC**

Size

Project Name

**KABINI**

Rev  
**SA**

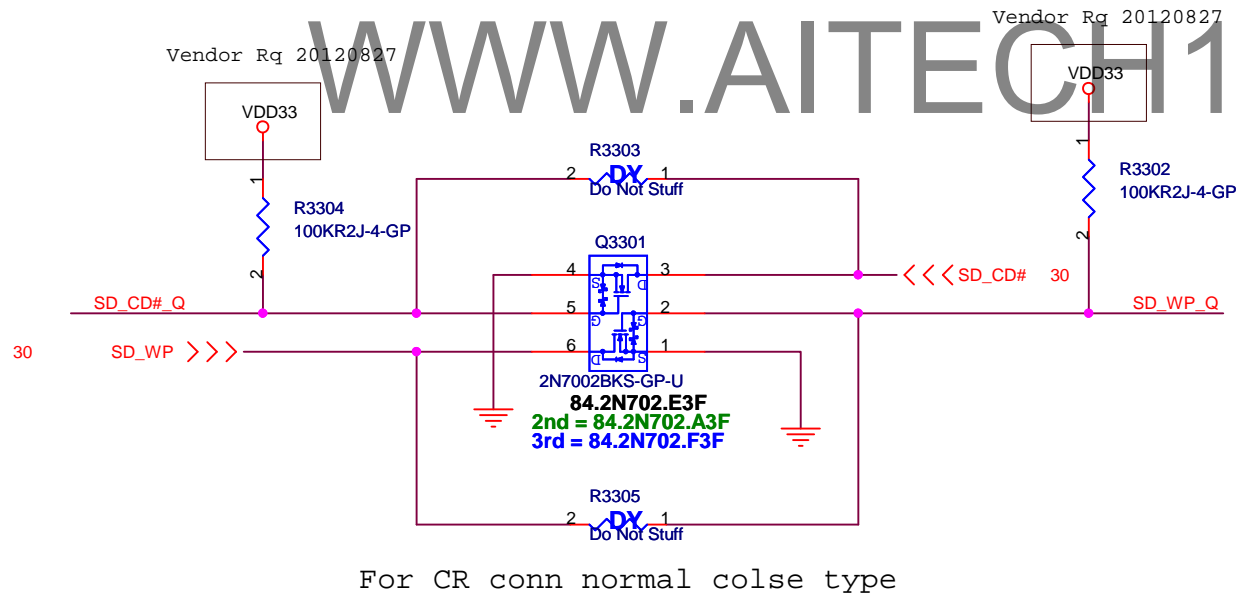
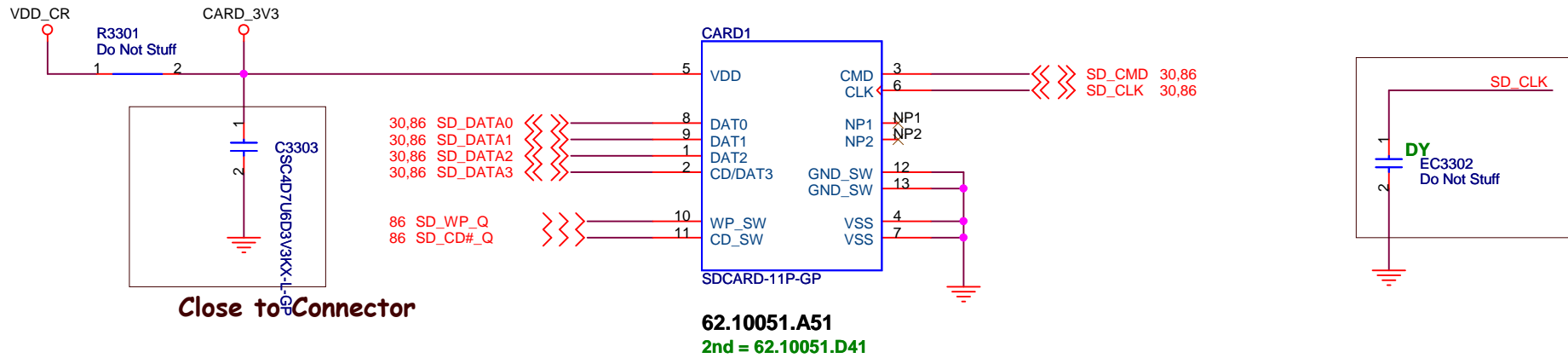
Date: Friday, September 07, 2012

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SSID = SDIO

# SD//MS Card Reader



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Title

**CARD Reader CONN**

Size

Project Name

**KABINI**

Rev

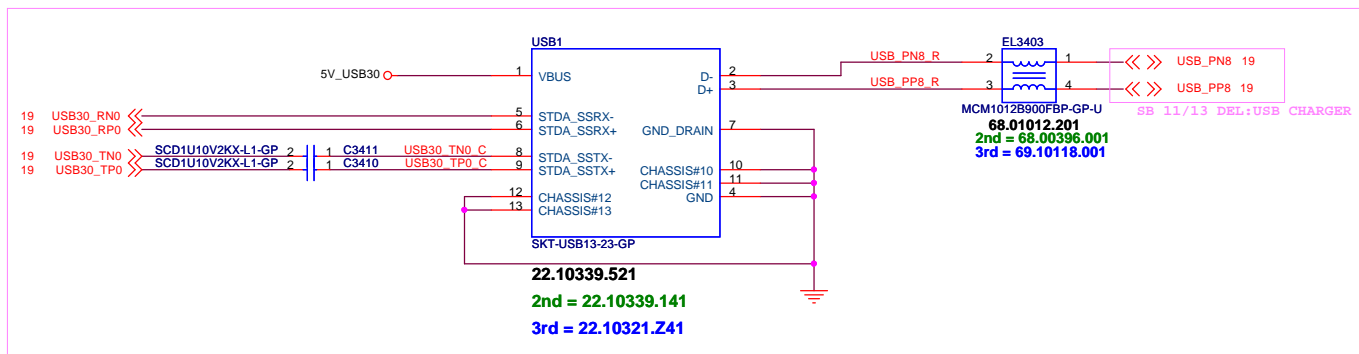
**SA**

Date: Monday, February 04, 2013

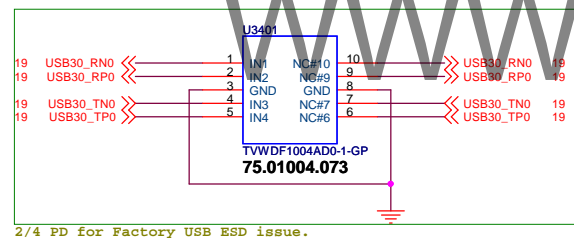
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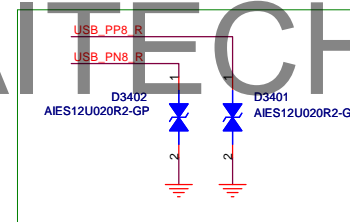
USB 2.0 CONTACT PIN		USB 3.0 CONTACT PIN	
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	VBUS	5	StdA_SSRX-
2	D-	6	StdA_SSRX+
3	D+	7	GND_DRAIN
4	GND	8	StdA_SSTX-
		9	StdA_SSTX+



SB 11/13 Change USB30 P/N

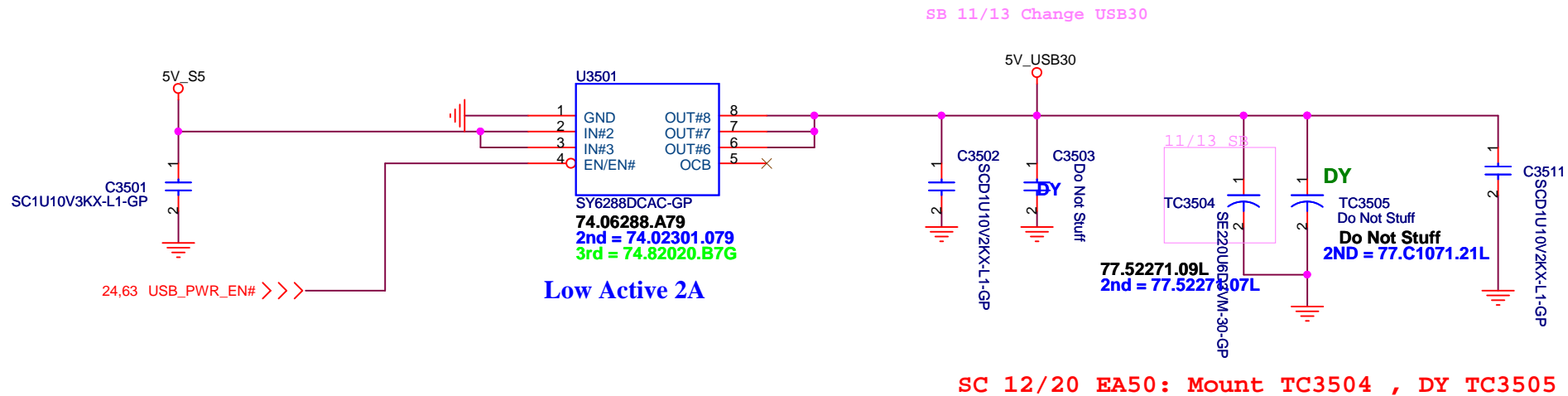


2/4 PD for Factory USB ESD issue.



1/28 PD for Factory USB ESD issue.





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Title

**USB\_Charger**

Size

Project Name

**KABINI**

Rev

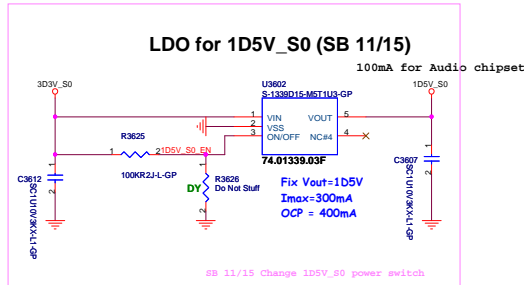
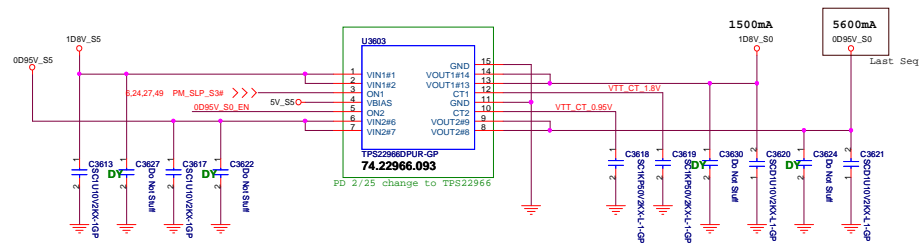
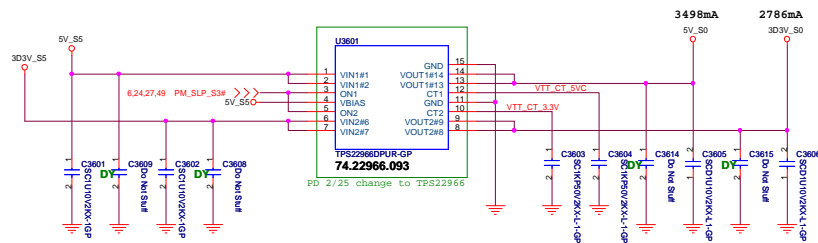
**SA**

Date: Monday, February 04, 2013

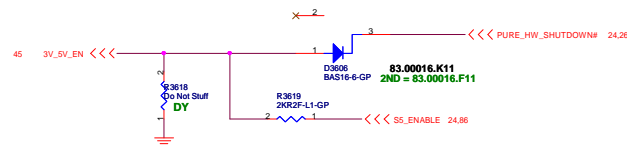
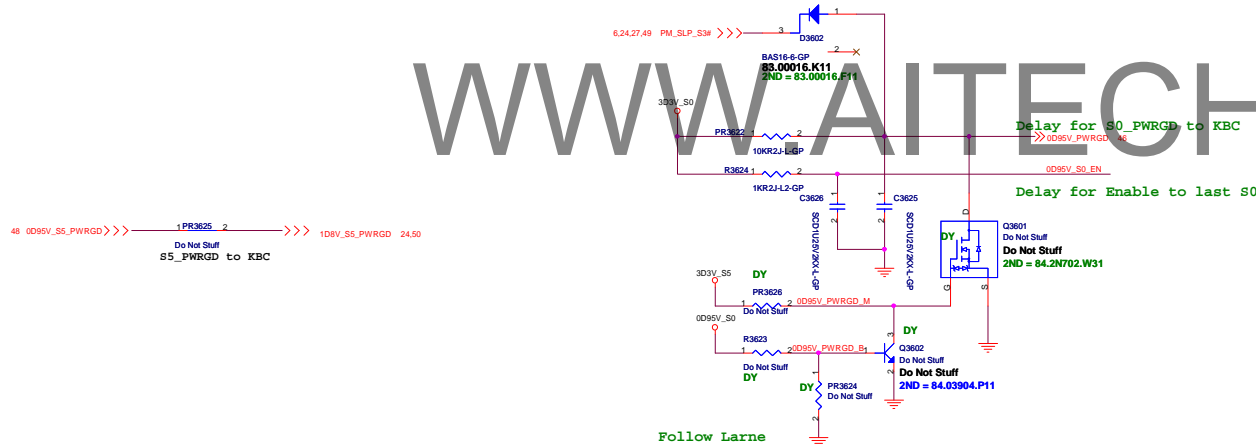
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# Power Sequence



WWW.AITECH1.RU



EAEG50 KB UMA

緯創資通		Wistron Corporation	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Power Plane Enable			
Size	Project Name		Rev
	KABINI		SA
Date:	Monday, February 25, 2013		Sheet 36 of 102



WWW.AITECH1.RU

EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**ADAPTER OCP / S3 reduction**

Size

Project Name

**KABINI**

Rev

**SA**

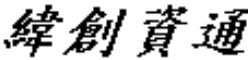
Date: Thursday, January 24, 2013

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WWW.AITECH1.RU

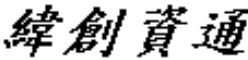
EAEG50 KB UMA

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Deep Standby			
Size	Project Name		Rev
	KABINI		SA
Date:	Friday, September 07, 2012		Sheet 38 of 102



WWW.AITECH1.RU

EAEG50 KB UMA

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D05_M			
Size	Project Name		Rev
	KABINI		SA
Date:	Friday, September 07, 2012	Sheet	39 of 102



WWW.AITECH1.RU

EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

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WWW.AITECH1.RU

EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Project Name

**KABINI**

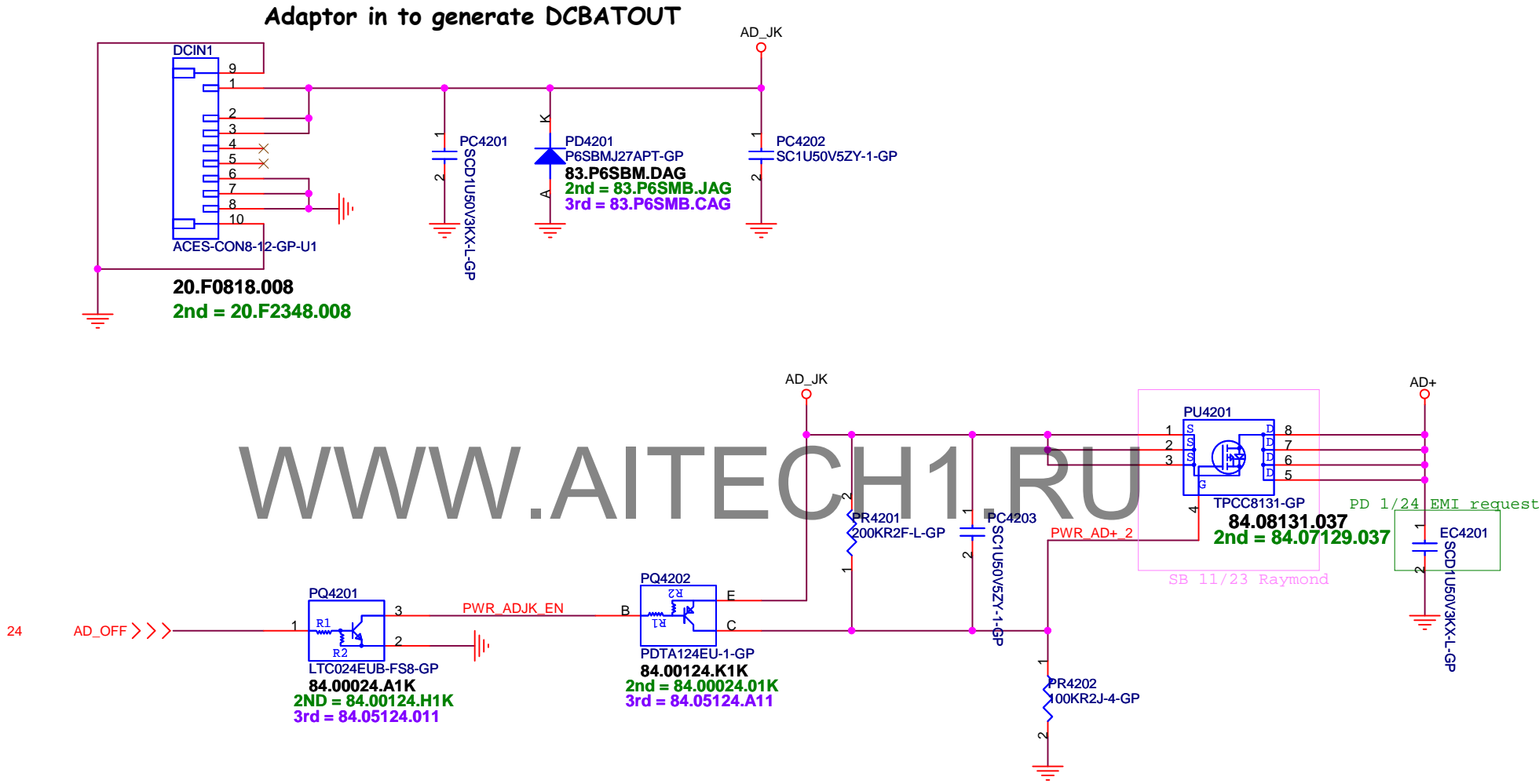
Rev

**SA**

Date: Friday, September 07, 2012

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86	BATA_SDA_1	>>	_____
86	BATA_SCL_1	>>	_____
86	BAT_IN#_1	>>	_____
86	BAT_G	>>	_____

The schematic diagram illustrates the internal circuitry of the AITECH1 module. Key components and their connections include:

- Power and Grounding:**
  - PC4301** (SCD1U50V3KX-L-GP) and **PC4302** (SC2K2P50V2KX-L-GP) are capacitors connected to the **BT+O** line and ground.
  - PG4301** (Do Not Stuff) is a component connected to the **BT+\_SENSE** line and ground.
  - PR4302** (Do Not Stuff) is a component connected to the **BAT\_G** line and ground.
- Communication and Control:**
  - PN4301** (SRN33J-7-GP-U) is a component connected to the **BAT\_IN#**, **BAT\_IN#\_1**, **BAT\_IN#\_2**, **BAT\_IN#\_3**, **BAT\_IN#\_4**, **BAT\_IN#\_5**, **BAT\_IN#\_6**, **BAT\_IN#\_7**, **BAT\_IN#\_8**, **BAT\_IN#\_9**, **BAT\_IN#\_10**, **BAT\_IN#\_11**, **BAT\_IN#\_12**, **BAT\_IN#\_13**, **BAT\_IN#\_14**, **BAT\_IN#\_15**, **BAT\_IN#\_16**, **BAT\_IN#\_17**, **BAT\_IN#\_18**, **BAT\_IN#\_19**, **BAT\_IN#\_20**, **BAT\_IN#\_21**, **BAT\_IN#\_22**, **BAT\_IN#\_23**, **BAT\_IN#\_24**, **BAT\_IN#\_25**, **BAT\_IN#\_26**, **BAT\_IN#\_27**, **BAT\_IN#\_28**, **BAT\_IN#\_29**, **BAT\_IN#\_30**, **BAT\_IN#\_31**, **BAT\_IN#\_32**, **BAT\_IN#\_33**, **BAT\_IN#\_34**, **BAT\_IN#\_35**, **BAT\_IN#\_36**, **BAT\_IN#\_37**, **BAT\_IN#\_38**, **BAT\_IN#\_39**, **BAT\_IN#\_40**, **BAT\_IN#\_41**, **BAT\_IN#\_42**, **BAT\_IN#\_43**, **BAT\_IN#\_44**, **BAT\_IN#\_45**, **BAT\_IN#\_46**, **BAT\_IN#\_47**, **BAT\_IN#\_48**, **BAT\_IN#\_49**, **BAT\_IN#\_50**, **BAT\_IN#\_51**, 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 <div> <b>Wistron Corporation</b>                  21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,                  Taipei Hsien 221, Taiwan, R.O.C.             </div>	
Title	
<div> <b>BATT CONN</b>  <b>KABINI</b> </div>	
Size	Project Name <div> <b>KABINI</b> </div>
	Rev <div> <b>SA</b> </div>
Date: Wednesday, February 20, 2013	Sheet 43 of 102



AD+ total power	R1	R2
65w 105%	18.7K	100K
90w	65k	100K

[illegible]

Battery OCP		R3	R4
6 Cell (3S2P)	8A	32.4K	49.9K
4 Cell (4S1P)	4.5A	95.3K	49.9K

Battery UVP		R5	R6
6 Cell (3S2P)	9V	78.7K	49.9K
4 Cell (4S1P)	12V	46.4K	49.9K



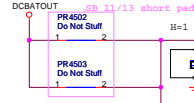
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Cut off itself

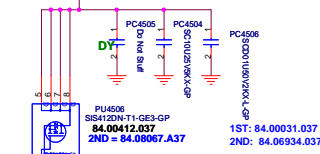
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check (DCBATOUT)

check (DCBATOUT)

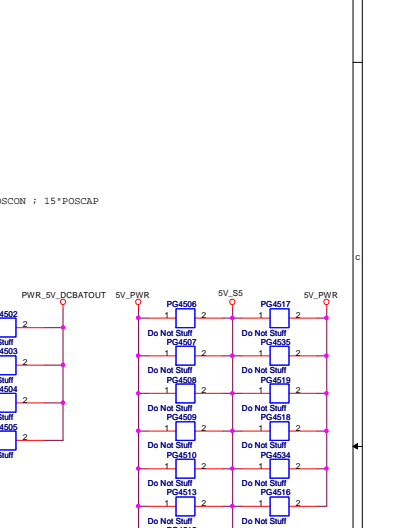
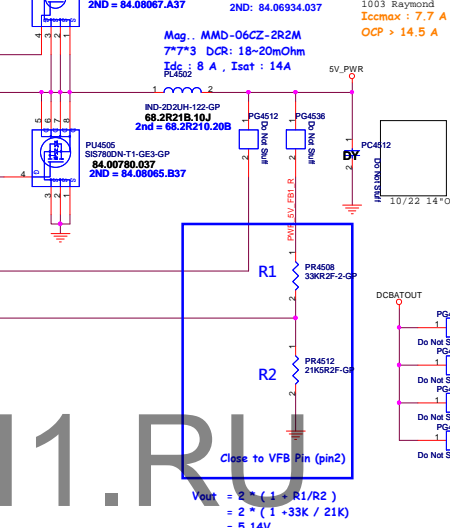
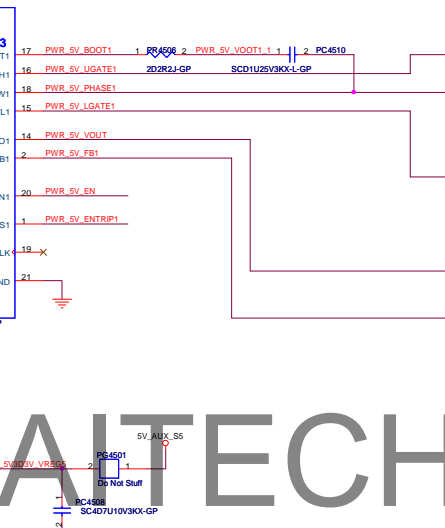
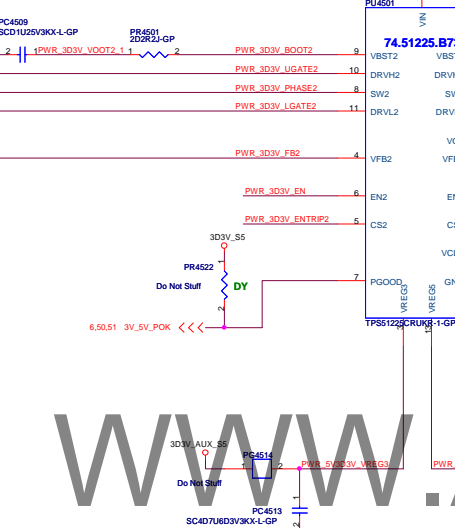
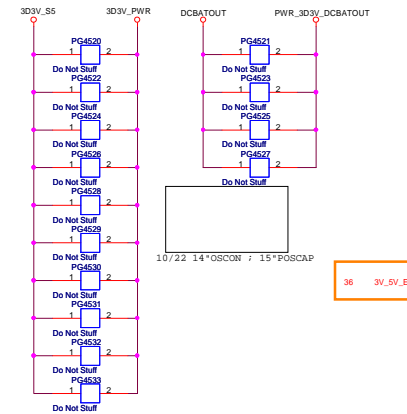
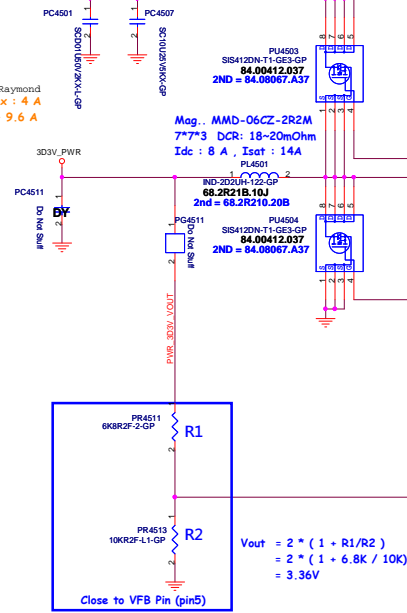


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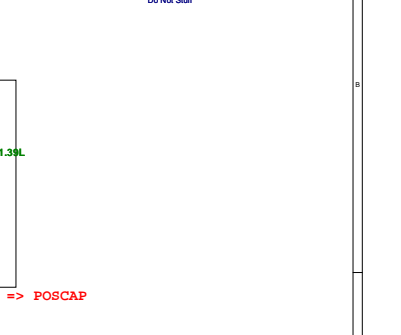
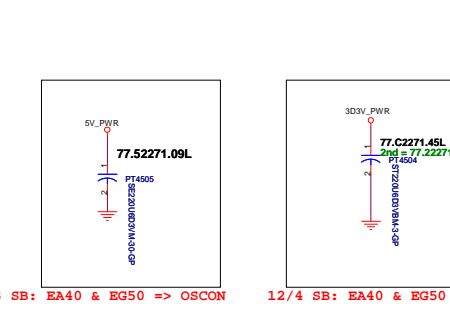
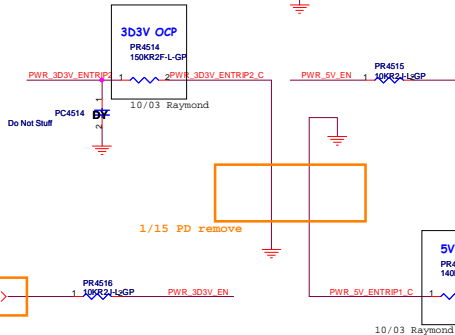


1003 Raymond  
Iccmax : 4 A  
OCP > 9.6 A

1003 Raymond  
Iccmax : 7.7 A  
OCP > 14.5 A



WWW.AITECH1.RU



EAE50 KB UMA

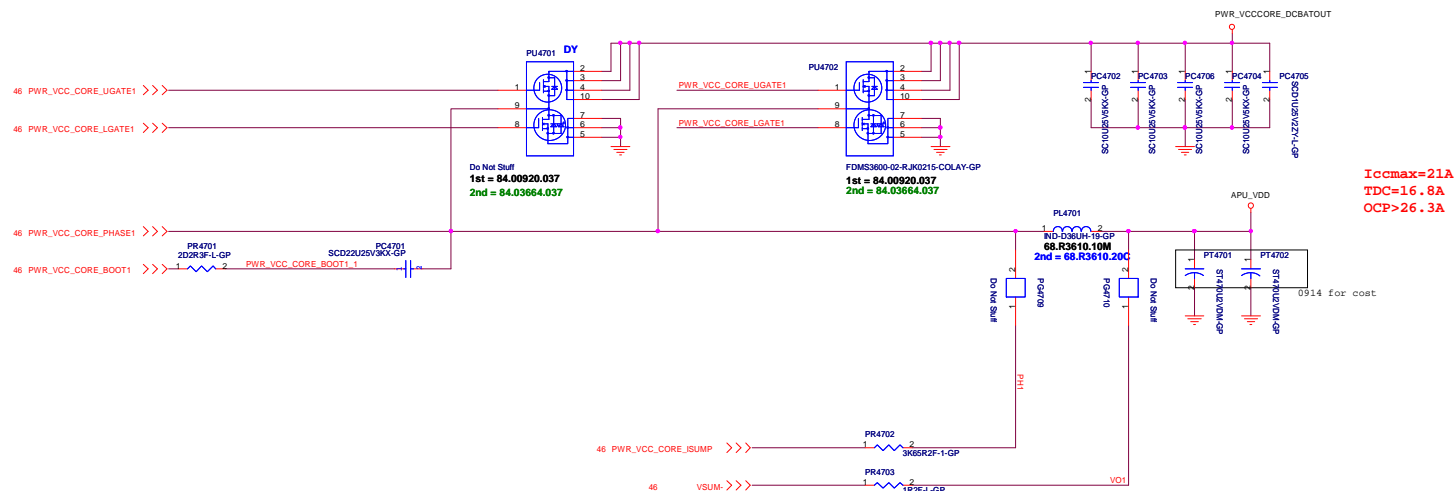
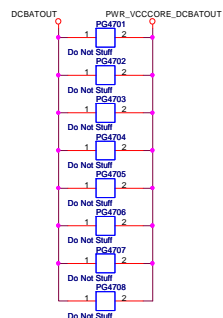
緯創資通 Wistron Corporation  
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsueh,  
Taipei Hsien 221, Taiwan, R.O.C.

TPS51225 5V/3D3V		
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Date: Monday, February 04, 2013		
Sheet	45	of 102

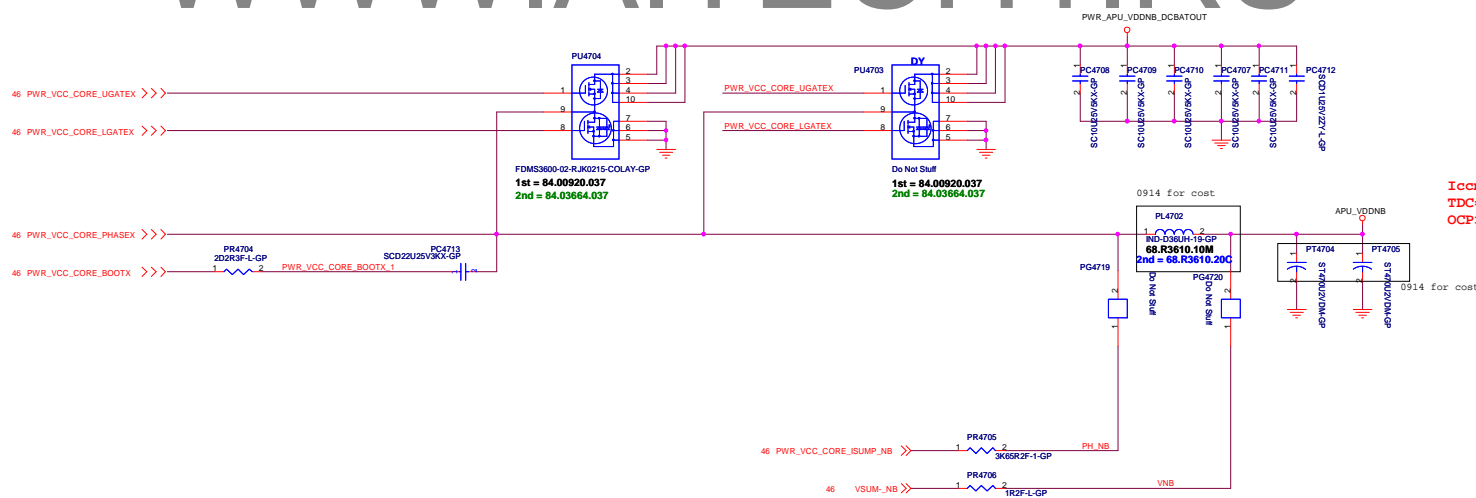
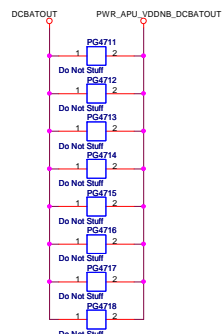




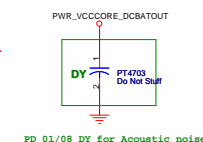




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TDC=16.8A  
OCP>26.3A



Iccmax=17A  
TDC=13.6A  
OCP>21.3A



WWW.AITECH1.RU

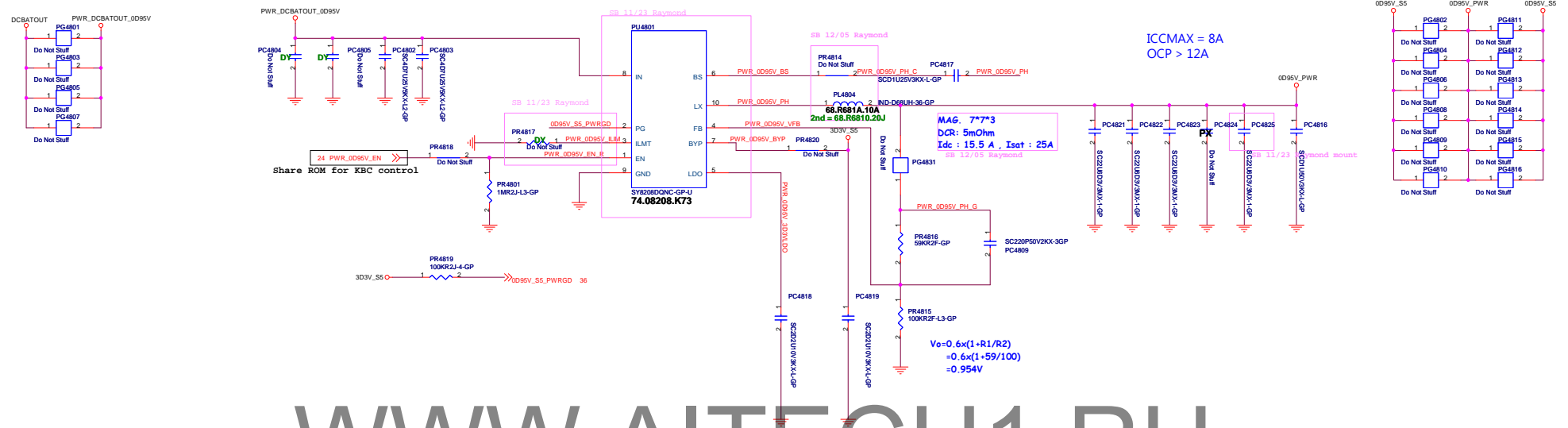
EAE650 KB UMA

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipai Hsien 221, Taiwan, R.O.C.

Title TPS51631 CPUCORE(2/2)  
Size A2 Document Number KABINI  
Date Monday, February 04, 2013 Sheet 47 of 102

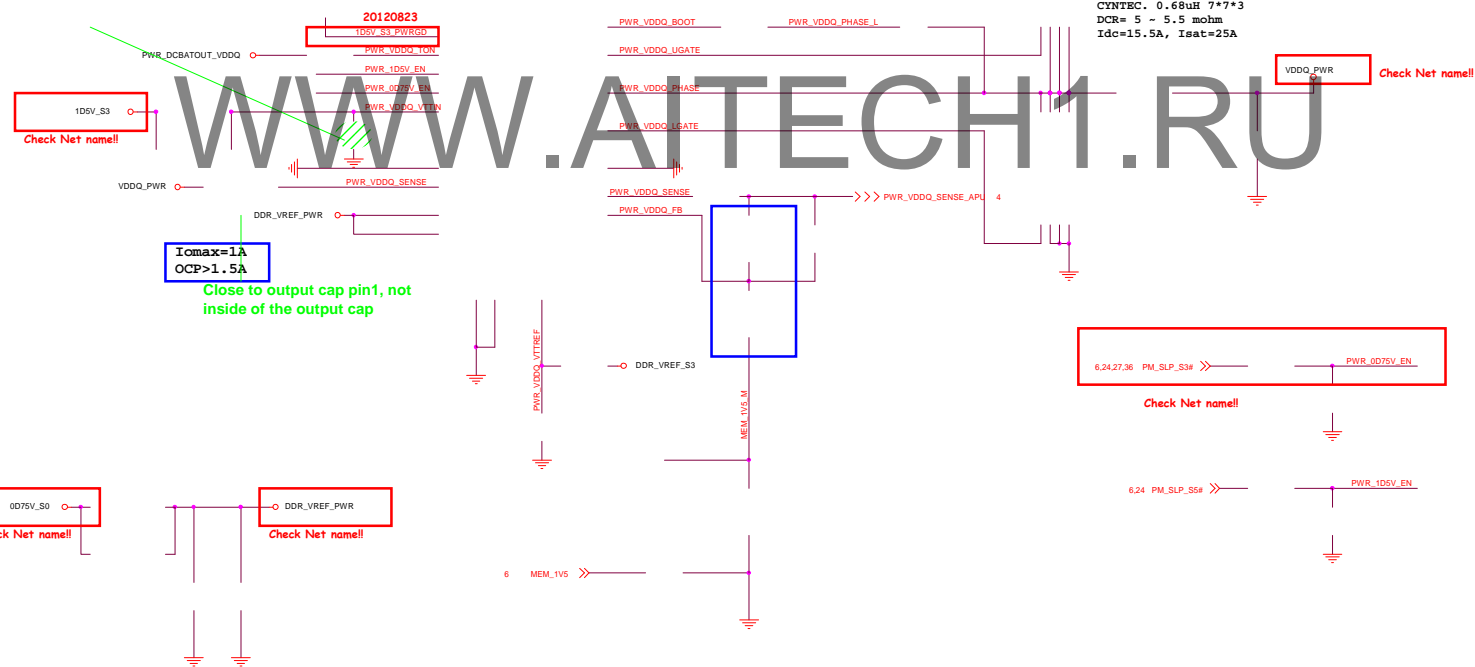
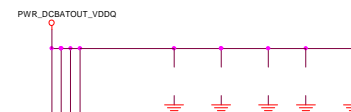
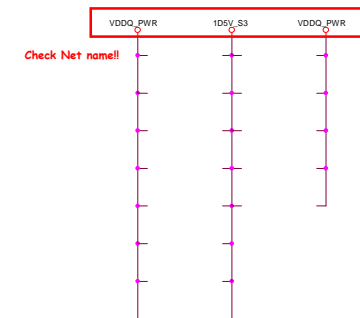


# SY8208D for 0D95V



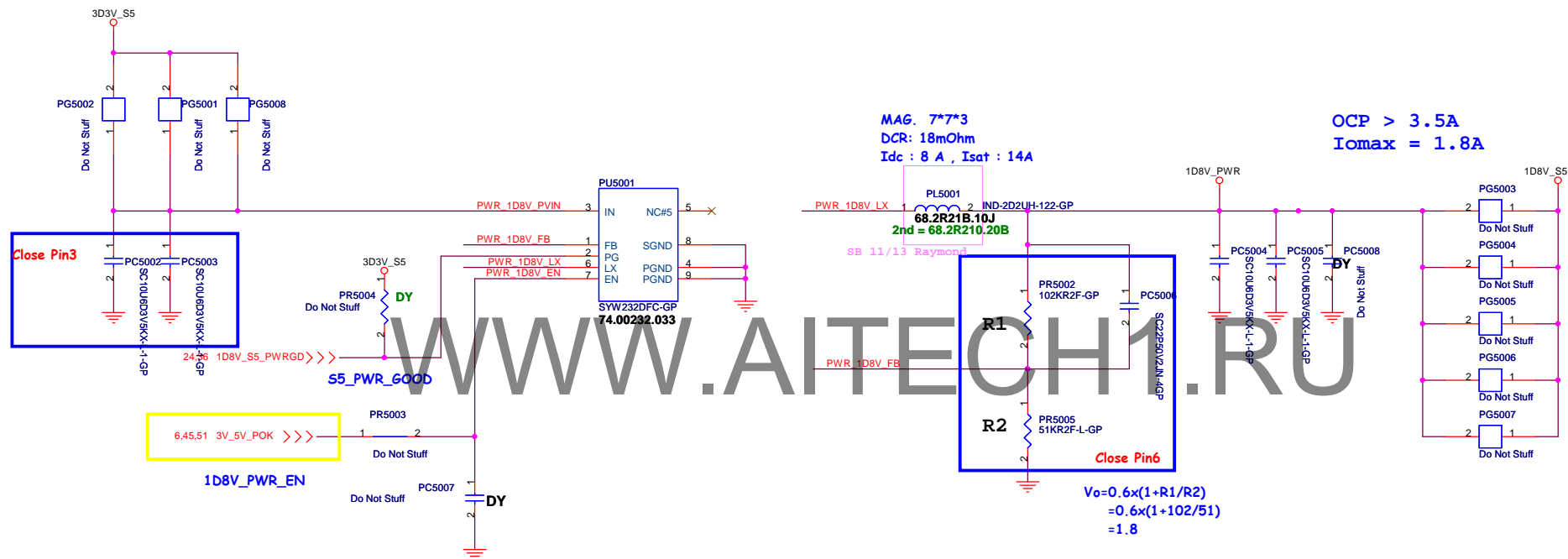
WWW.AITECH1.RU







```
SSID = PWR.Plane.Regulator_1p8v
```



EAEG50 KB UMA

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

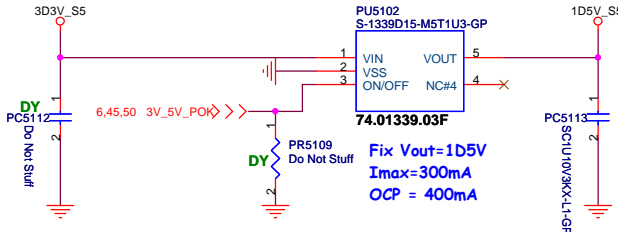
Title	1D8V_S0 SYW232
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Size A3	Document Number <b>KABINI</b>	Rev
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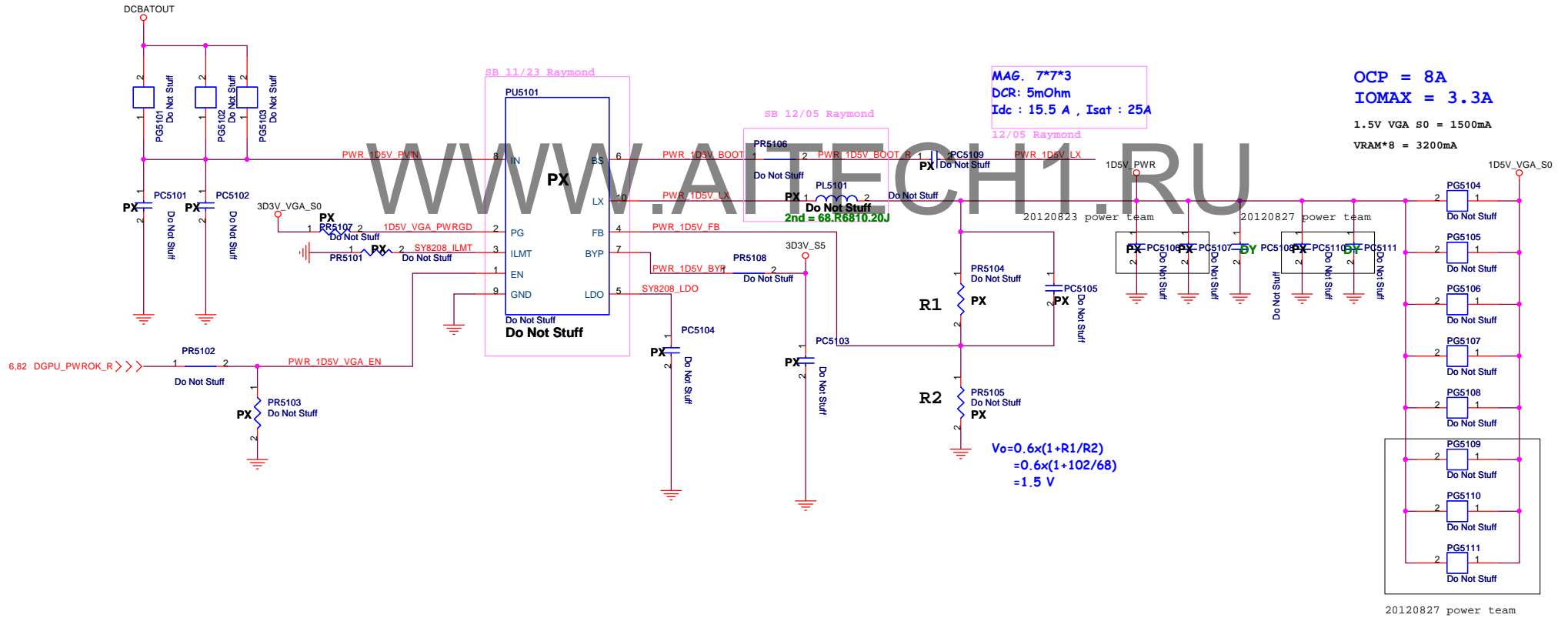
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## LDO for 1D5V\_S5 (SB 11/13)

$$1.5V \text{ S0} = 100mA(VDDIO\_AZ) + 100mA(Audio) + 600mA(Minicard \text{ DY}) = 200mA$$


## SY8208D for 1D5V\_VGA\_S0 (SB 11/13)



20120827 power team

**EAEG50 KB UMA**

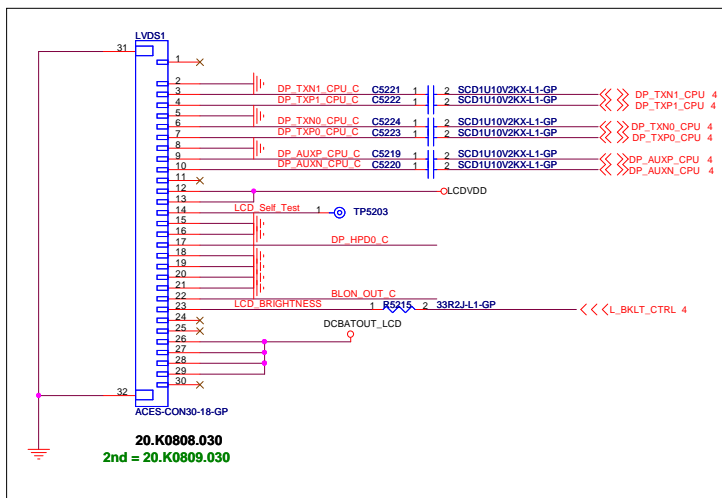
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title				<b>1D5V_S5 SY8208D</b>			
Size	Document Number					Rev	
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Date:	Tuesday, February 19, 2013			Sheet	51	of	102



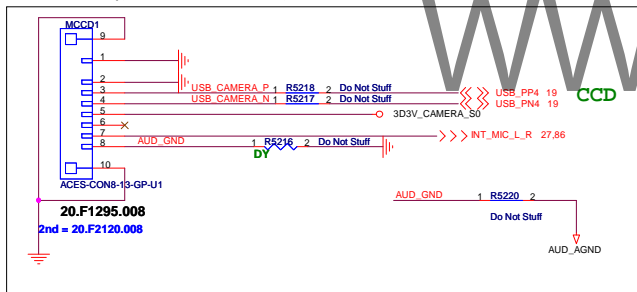
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## eDP Conn.



10/04 change to 20.K0808.030 for ME request

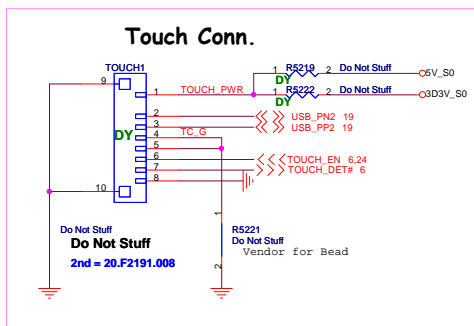
## Camera+MIC Conn.



10/03 change to 8pin for del DMIC

10/15 change to 20.F1295.008 follow HW

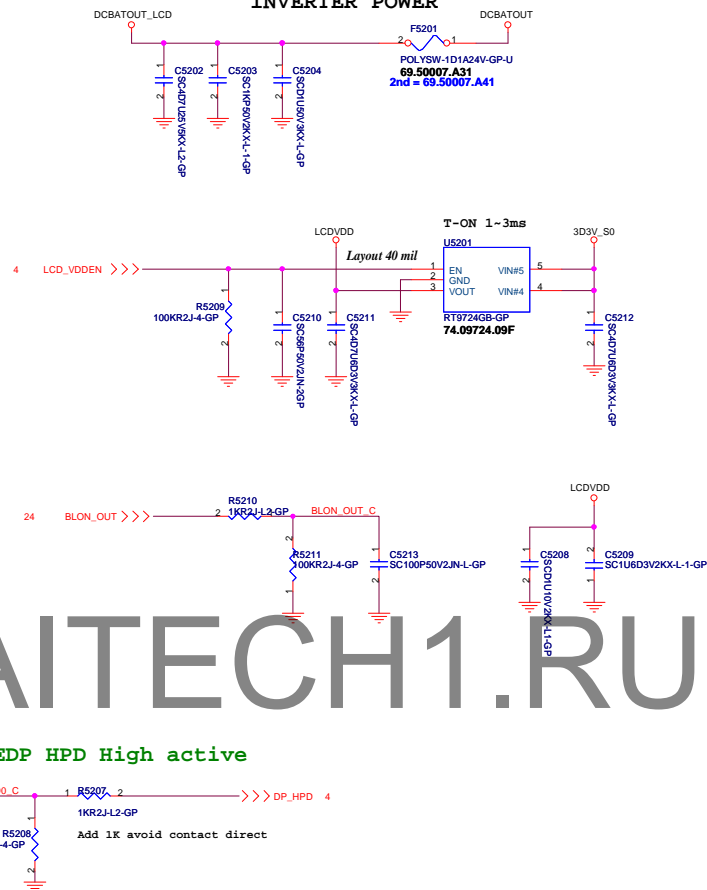
## Touch Conn.



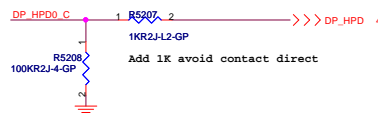
SB 12/12 DUMMY for ME issue

SC NO support

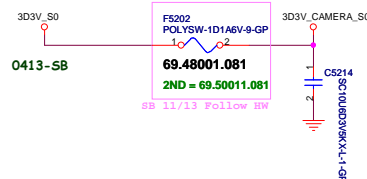
## INVERTER POWER



## EDP HPD High active



## Camera Power



86 AUD\_GND <<<

86 DP\_HPD0\_C >>>

86 BLON\_OUT\_C >>>

86 LCD\_BRIGHTNESS >>>

86 DP\_TXN1\_CPU\_C >>>

86 DP\_TXP1\_CPU\_C >>>

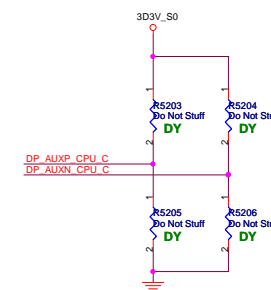
86 DP\_TXN0\_CPU\_C >>>

86 DP\_TXP0\_CPU\_C >>>

86 DP\_AUXP\_CPU\_C <<<

86 DP\_AUXN\_CPU\_C <<<

For AFTE



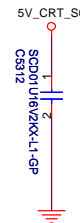
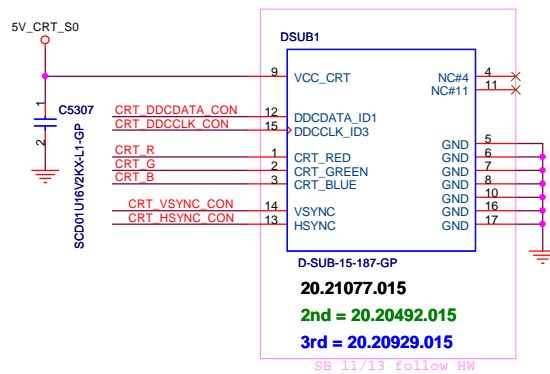
EAEG50 KB UMA

緯創資通

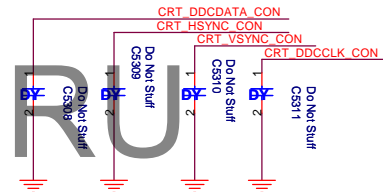
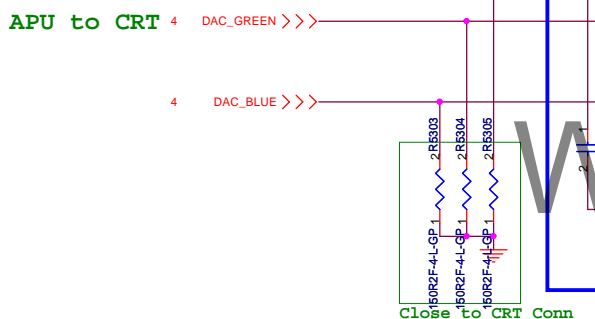
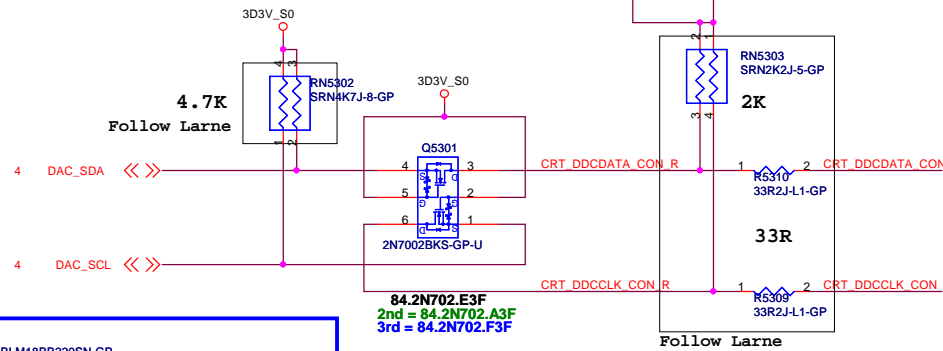
Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD Connector		
Size	Project Name	Rev
	KABINI	SA
Date: Monday, February 25, 2013		
Sheet 52 of 102		



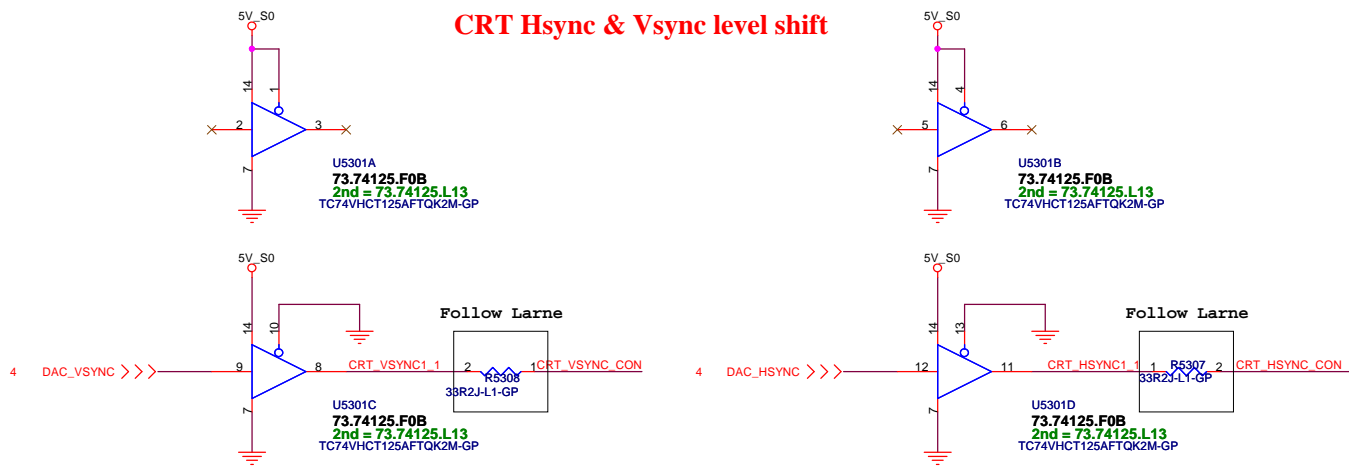


## CRT DDCDATA & DDCCLK level shift



10/16 follow COMAL

## CRT Hsync & Vsync level shift



EAEG50 KB UMA

緯創資通 Wistron Corporation

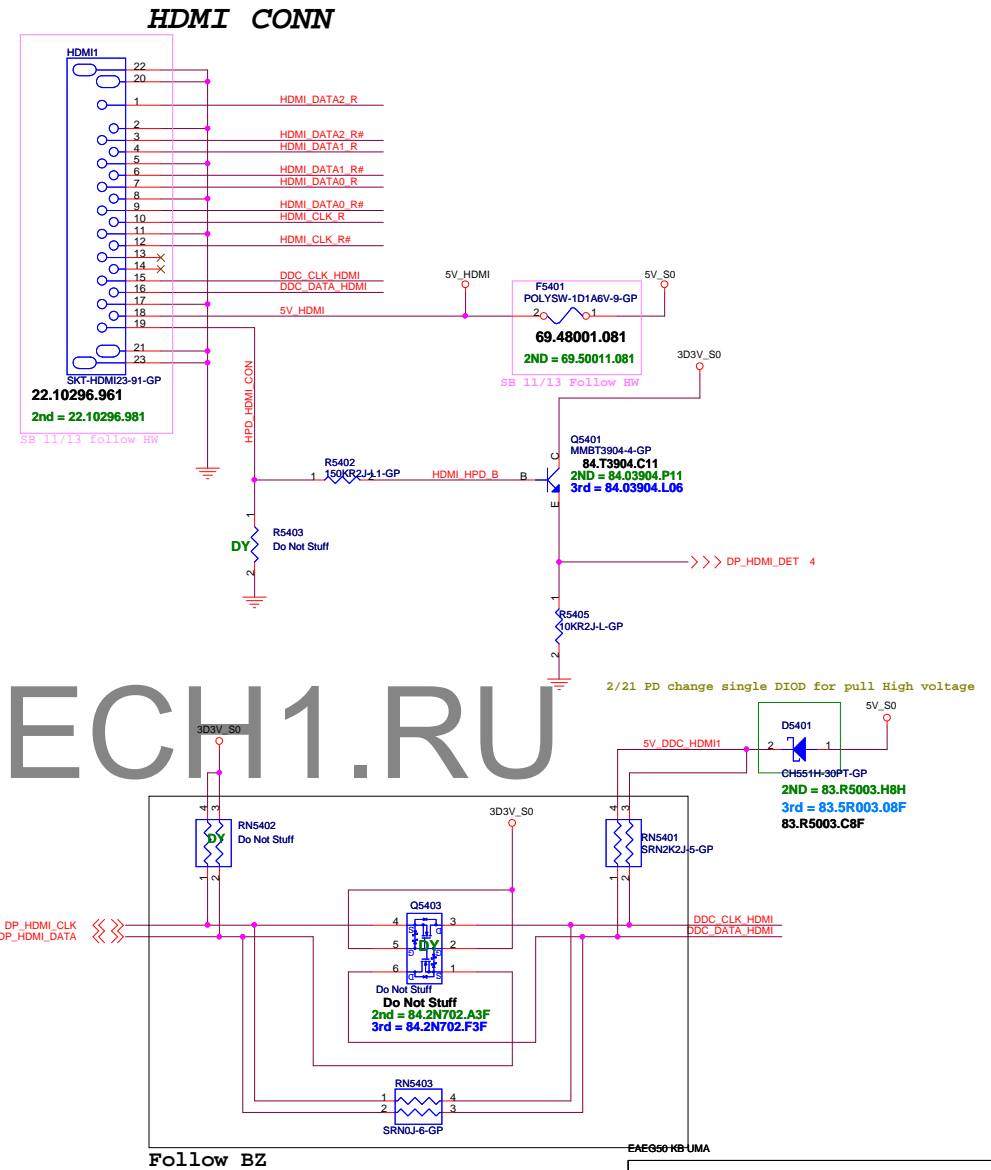
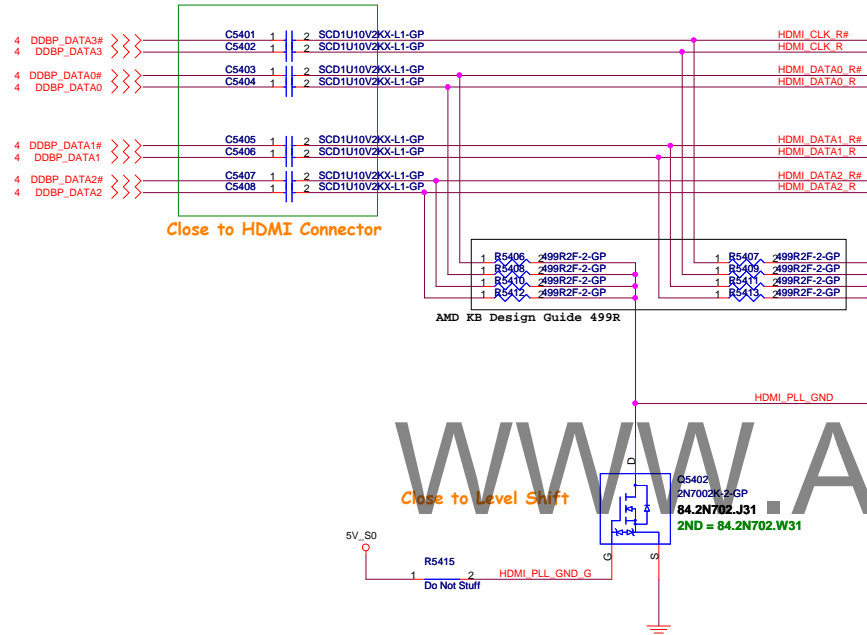
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Board Connector		
Size	Project Name	Rev
	KABINI	SA
Date: Monday, February 04, 2013		
Sheet	53	of 102



SSID = VIDEO

# HDMI Level Shifter & CONNECTOR



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HDMI Level Shifter/Connector			
Size	Project Name	KABINI	Rev SA
Date	Thursday, February 21, 2013	Sheet 54	of 102



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**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size

Project Name

**KABINI**

Rev

**SA**

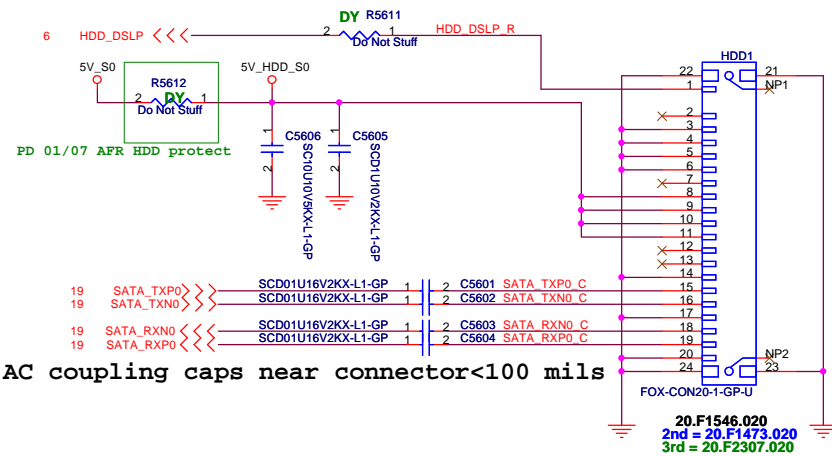
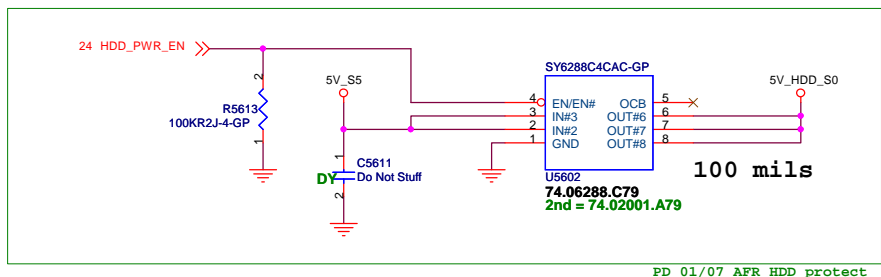
Date: Friday, September 07, 2012

Sheet 55 of 102



SSID = SATA

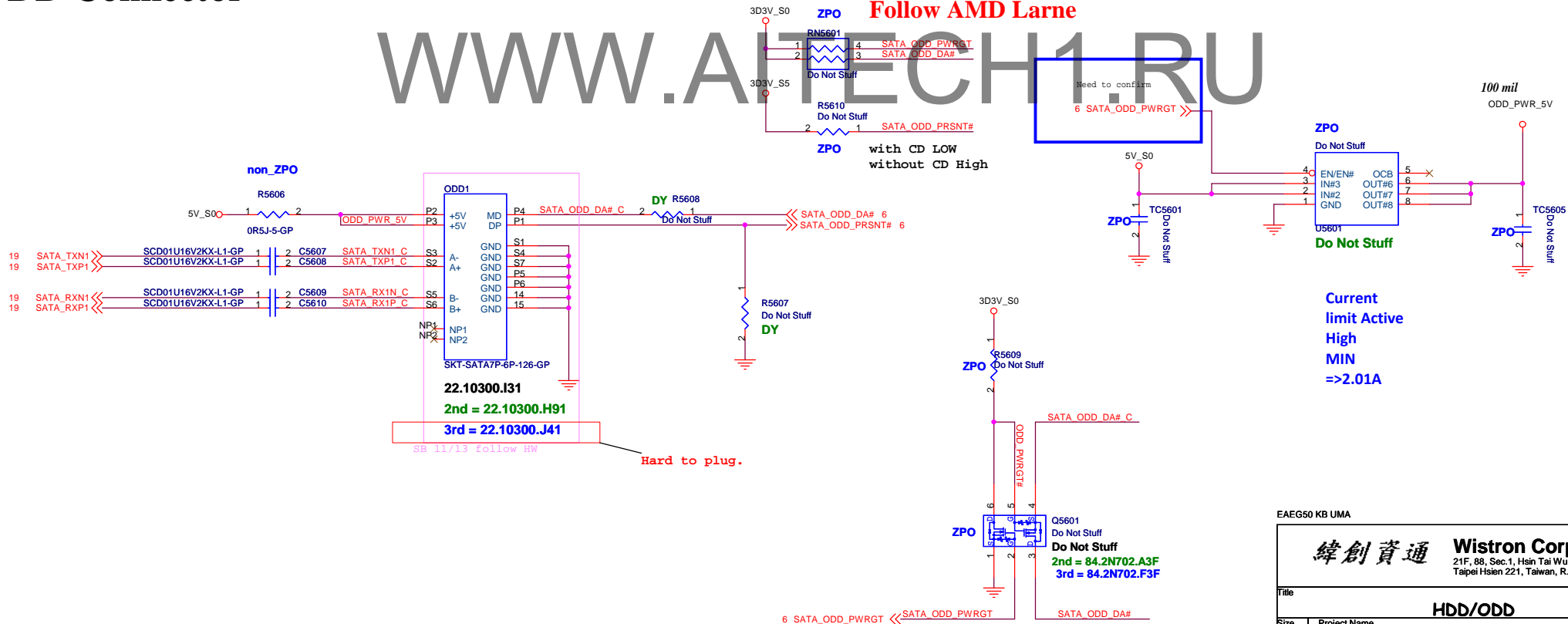
# SATA HDD Connector



# ODD Connector

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SATA Zero Power ODD  
Follow AMD Larne





WWW.AITECH1.RU

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Title

**Reserved**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

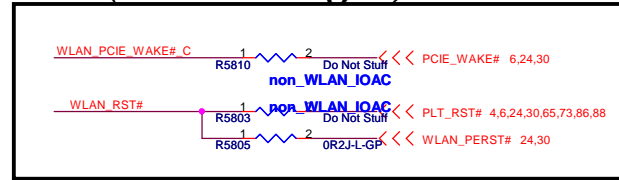
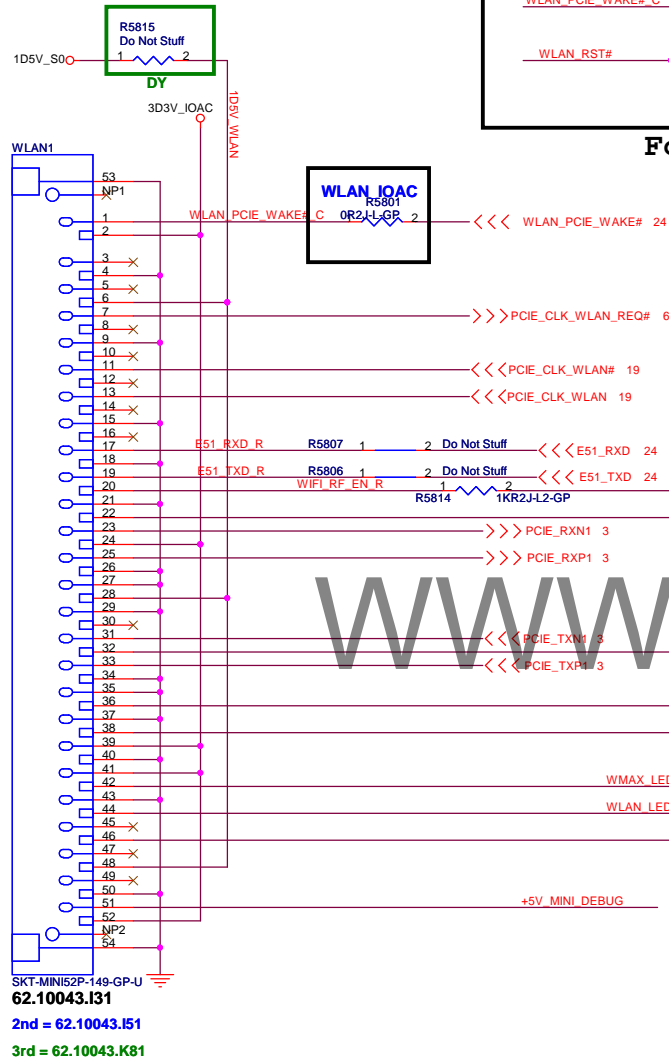
Sheet 57 of 102



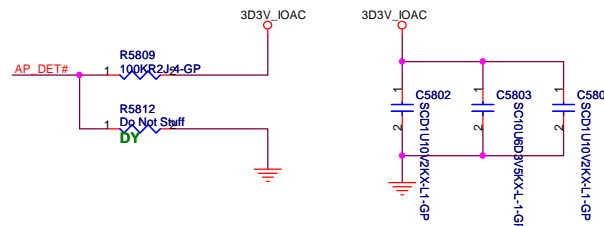
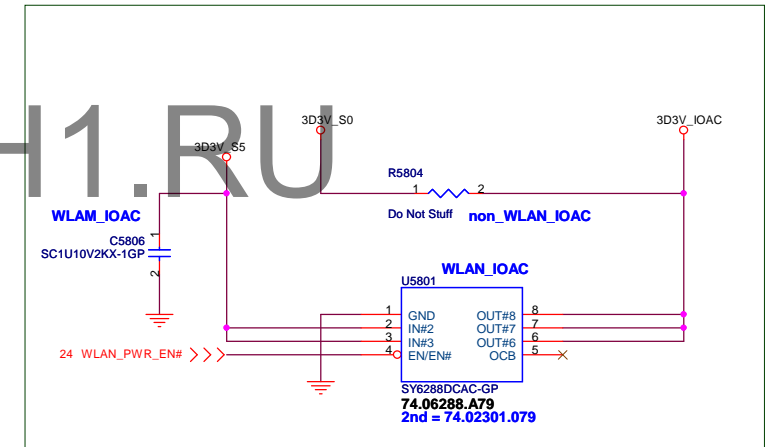
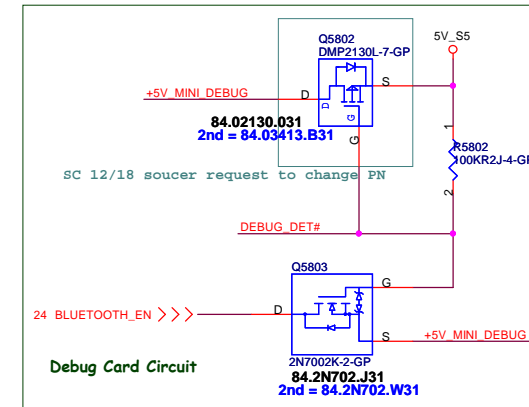
SSID = Wireless

# Mini Card Connector(802.11a/b/g/n)

10/15 follow EA40-HW



Follow VP40



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緯創資通 Wistron Corporation

Title			MINICARD(WLAN)
Size	Project Name	KABINI	
Date:	Tuesday, February 19, 2013	Sheet	58 of 102



SSID = Wireless

# Mini Card Connector(WWAN)

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Title

**WWAN CONN**

Size

Project Name

**KABINI**

Rev

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SSID = mSATA

Mini Card Connector(mSATA)

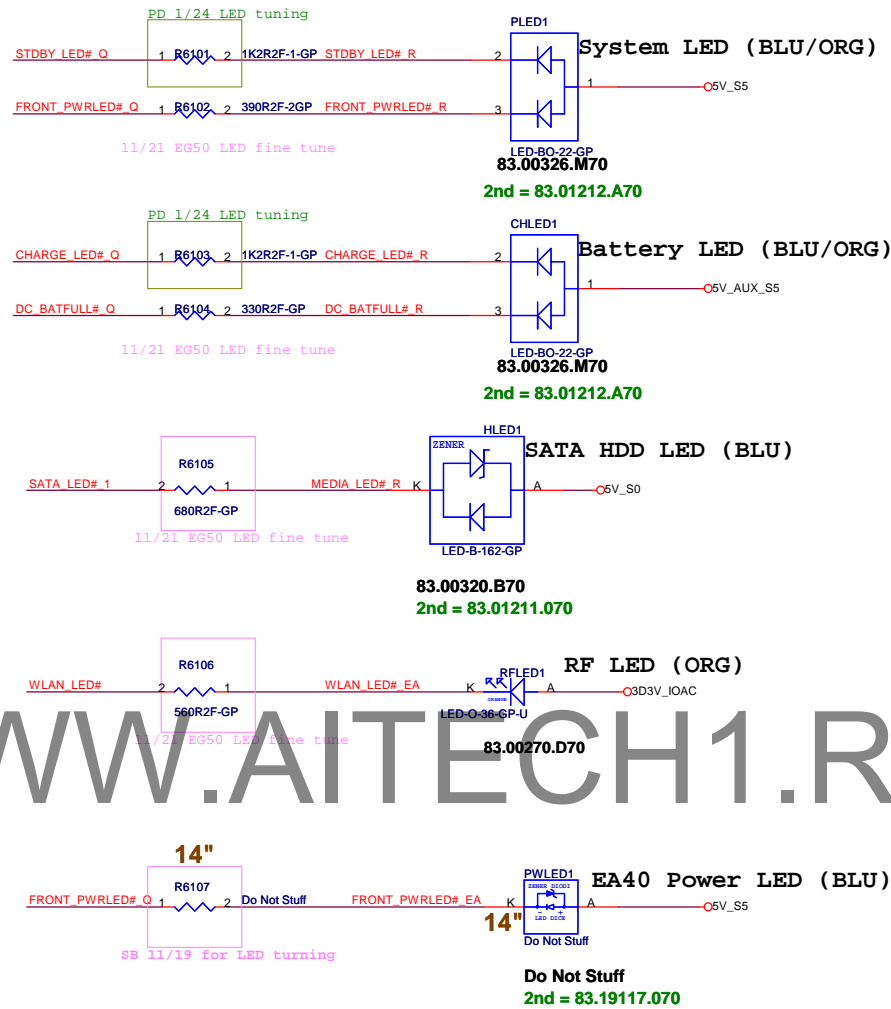
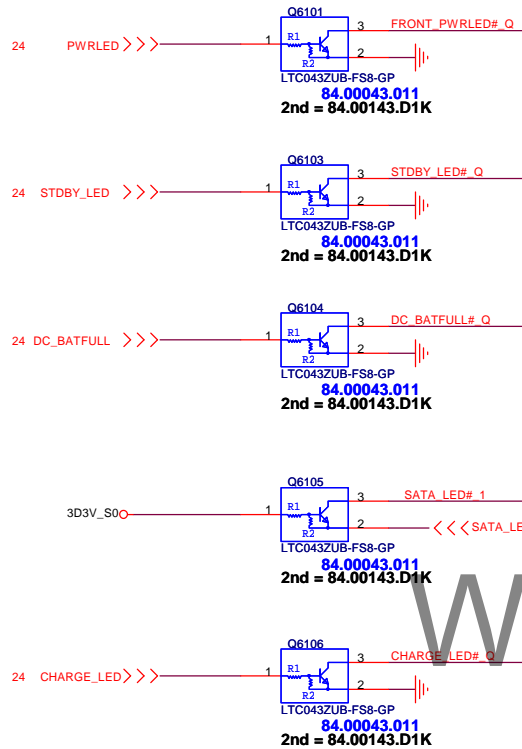
WWW.AITECH1.RU

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title mSATA Connector		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 60 of 102

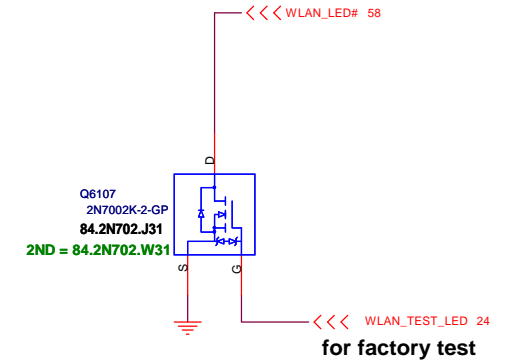


# SSID = User.Interface

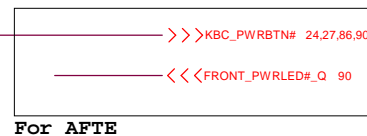
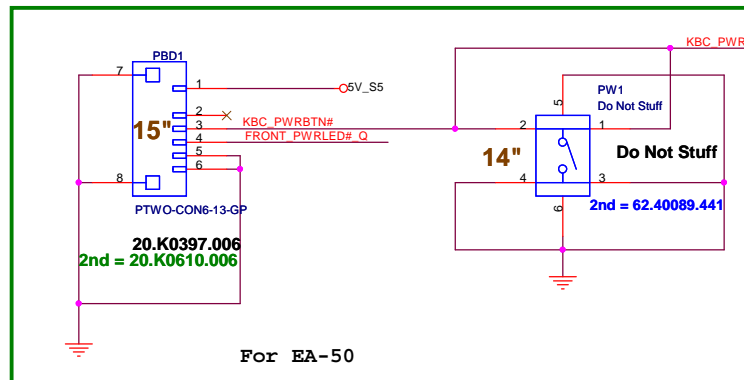
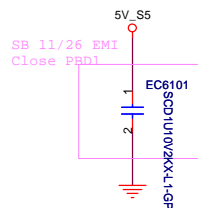


## WLAN\_LED

From module



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
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Title				
LED Bard/Power Button				
Size	Project Name			Rev
	KABINI			SA
Date:	Monday, February 04, 2013		Sheet 61 of 102	

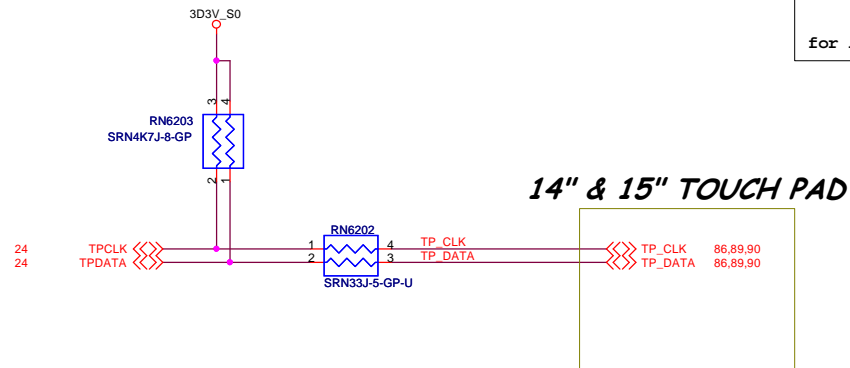


SSID = KBC

# Internal KeyBoard Connector

86,89,90 TP\_DATA >>>  
86,89,90 TP\_CLK >>>  
86,89,90 SWR >>>  
86,89,90 SWL >>>

for AFTP



PD 1/14 Different 14" & 15" TOUCH PAD reversion

14"& 15" use the same KB

### for EA/EG-50 ###

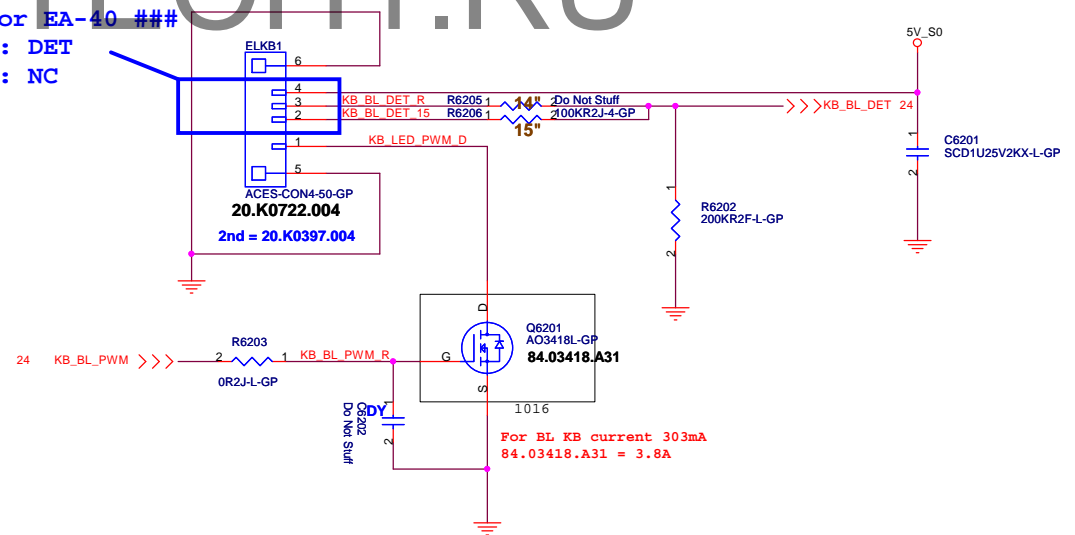
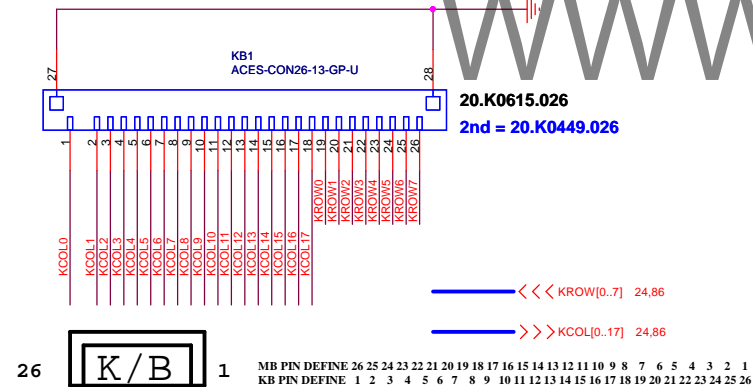
Pin3 : NC

Pin2 : DET

### for EA-40 ###

Pin3 : DET

Pin2 : NC



EAEG50 KB UMA

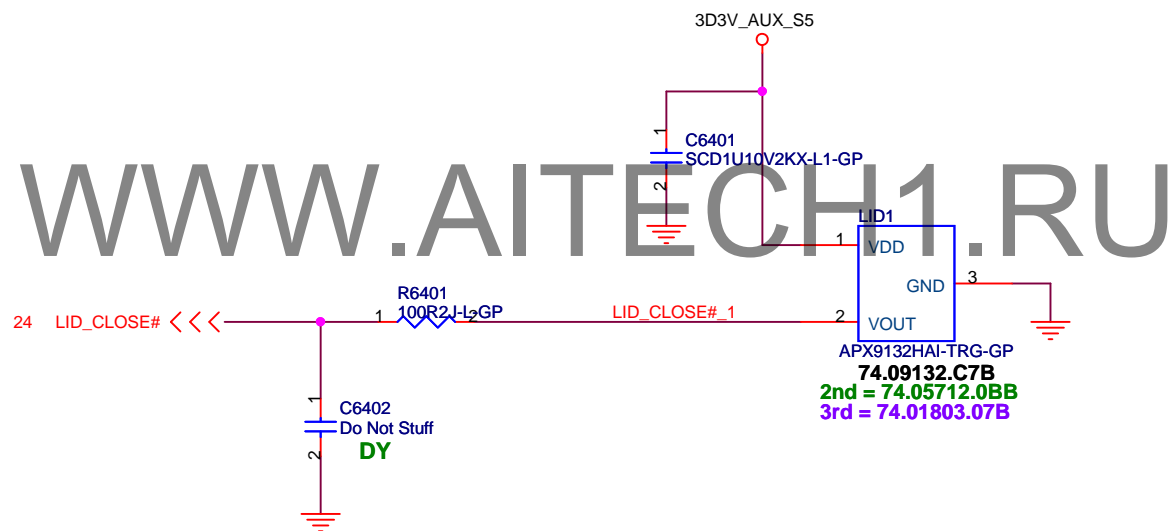
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Key Board/Touch Pad			
Project Name		KABINI	
Date: Tuesday, February 19, 2013		Sheet 62 of 102	









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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Hall Sensor**

Size

Project Name

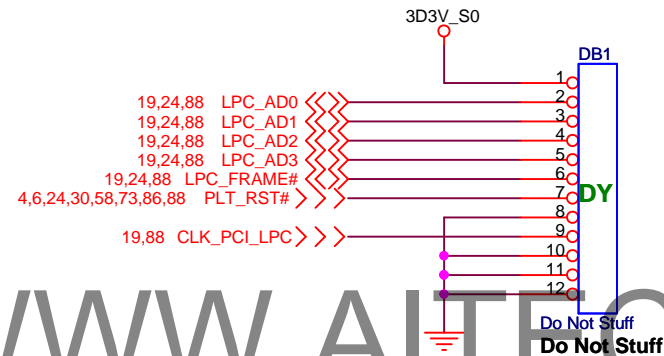
**KABINI**

Rev  
**SA**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Dubug connector**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Monday, February 04, 2013

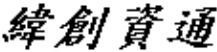
Sheet 65 of 102



(Blanking)

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EAEG50 KB UMA

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Reserved</b>			
Size	Project Name <b>KABINI</b>		Rev <b>SA</b>
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SSID = User.Interface

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Title			
<b>G Sensor</b>			
Size	Project Name		Rev
	<b>KABINI</b>		<b>SA</b>
Date: Friday, September 07, 2012		Sheet	67 of 102



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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt (1/5)**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt (2/5)**

Size

Project Name

**KABINI**

Rev

**SA**

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緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt (3/5)**

Size

Project Name

**KABINI**

Rev

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緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt (4/5)**

Size

Project Name

**KABINI**

Rev

**SA**

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EAEG50 KB UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Thunderbolt (5/5)**

Size

Project Name

**KABINI**

Rev

**SA**

Date: Friday, September 07, 2012

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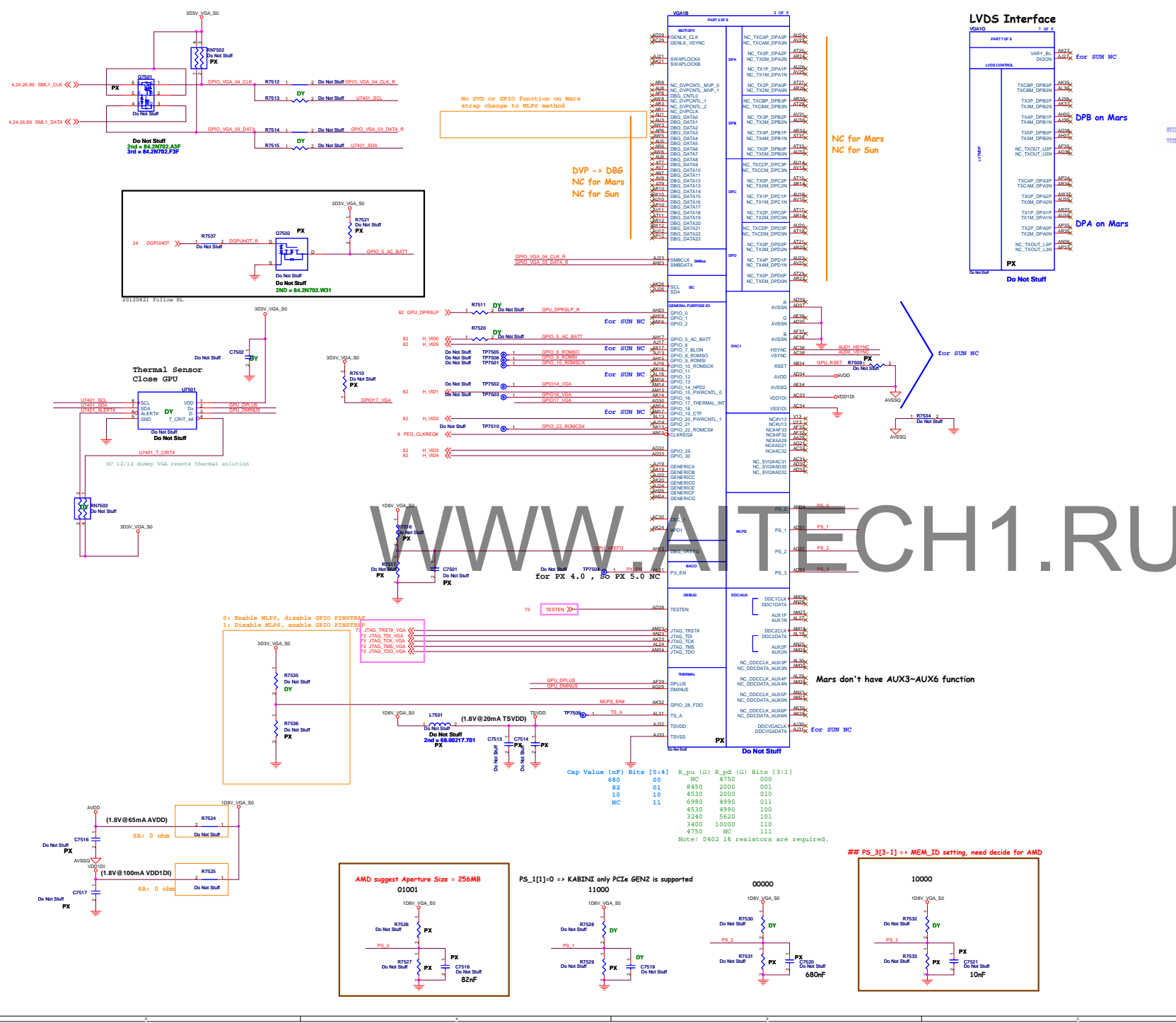












MLPS has setted AUD[1] and AUD[0] but these two strap also need to set

00 = 30 audio function  
01 = Audio for DP only  
10 = Audio for DP and HDMI if single is detected  
11 = Audio for both DP and HDMI  
HDMI must only be enabled on system that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

Table 3-11 Multi-Line Pin Straps

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1]	ROM_CONFIG[0]	If STRAP_ROM_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_0[0]	ROM_CONFIG[1]	If STRAP_ROM_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size. See Primary Memory Aperture Size (p. 68).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[3]	AUD_PORT_CON[0]	The L33 (Audio) register bit of the strap option that indicates the enable of audio-capable display output.	Design dependent, see the description.
PS_1[11]	STRAP_BIF_GEN2_ENLA	PCIe GEN2 capability. 1 = PCIe GEN2 is supported. 0 = PCIe GEN2 is not supported.	Design dependent, see the description.
PS_1[23]	STRAP_BIF_CLK_P0_EN	Determines whether or not the PCIe reference clock power management capability is supported in the PCIe configuration space (reference to PCIe CLP32[0]). 1 = The CLP32[0] power management capability is disabled. 0 = The CLP32[0] power management capability is enabled.	0
PS_1[31]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[41]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-swing mode. 0 = The transmitter full-swing is enabled. 1 = The transmitter full-swing is disabled.	1
PS_1[51]	STRAP_TX_DEEPEN_EN	PCI EXPRESS 5.0 transmitter, deepenable enable. 0 = Tx deepenable disabled. 1 = Tx deepenable enabled.	Design dependent, see the description.
PS_2[11]	N/A	Reserved.	N/A
PS_2[21]	N/A	Reserved.	N/A
PS_2[31]	STRAP_ROM_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
MLPS Bit	Strap Name	Description	Recommended Settings
PS_2[30]	STRAP_BIF_VGA_DIS	VGA disable. Determines whether or not the card will be recognized as the system's VGA controller. Through the DDC/CLP32 field in the PCI configuration space. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[39]	N/A	Reserved.	N/A
PS_3[1]	BOARD_CONFIG[0]	Board configuration related wrapping, such as for memory ID.	Design dependent, see the description.
PS_3[2]	BOARD_CONFIG[1]	Board configuration related wrapping, such as for memory ID.	Design dependent, see the description.
PS_3[3]	BOARD_CONFIG[2]	Board configuration related wrapping, such as for memory ID.	Design dependent, see the description.
PS_3[4]	AUD_PORT_CON[0]	Determines the maximum number of digital display audio outputs that will be presented to the OS and user. That should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC pins (small, the number and type of recovery on the board (DP, HDMI), and the number of audio for each DP connector (the DP-HDMI bit of the video driver). Cleared endpoints should be disabled. This pin strap is intended as an active low binary as follows to ensure zero enable all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 010 = Four usable endpoints. 011 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.
PS_3[5]	AUD_PORT_CON[1]	Determines the maximum number of digital display audio outputs that will be presented to the OS and user. That should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC pins (small, the number and type of recovery on the board (DP, HDMI), and the number of audio for each DP connector (the DP-HDMI bit of the video driver). Cleared endpoints should be disabled. This pin strap is intended as an active low binary as follows to ensure zero enable all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 010 = Four usable endpoints. 011 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.
PS_3[6]	AUD_PORT_CON[2]	Determines the maximum number of digital display audio outputs that will be presented to the OS and user. That should be set to the maximum number of digital display audio outputs that can be enabled simultaneously in the product, which is limited by the ASIC pins (small, the number and type of recovery on the board (DP, HDMI), and the number of audio for each DP connector (the DP-HDMI bit of the video driver). Cleared endpoints should be disabled. This pin strap is intended as an active low binary as follows to ensure zero enable all endpoints. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 010 = Four usable endpoints. 011 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	Design dependent, see the description.

Note: AUD[1] (on BYSN) and AUD[0] (on VSYN) still need to be properly pin strapped even in a MLPS-based design.

EAE050 KB LMA

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Rev. 1.0  
Date: Tuesday, February 19, 2013  
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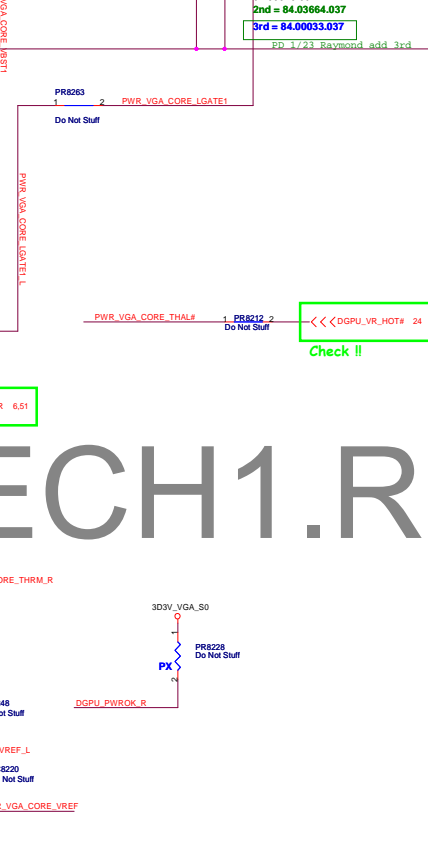
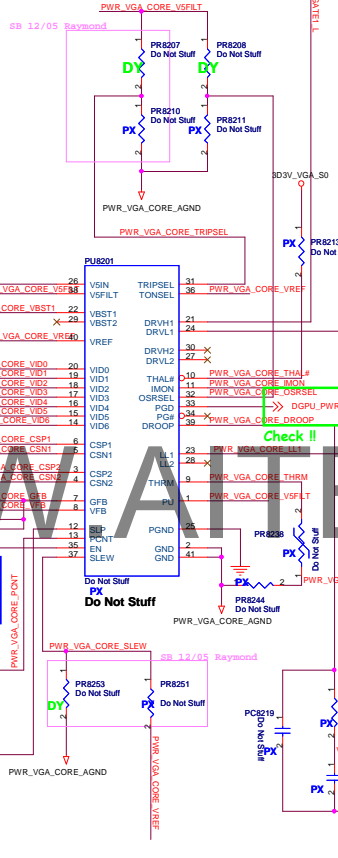
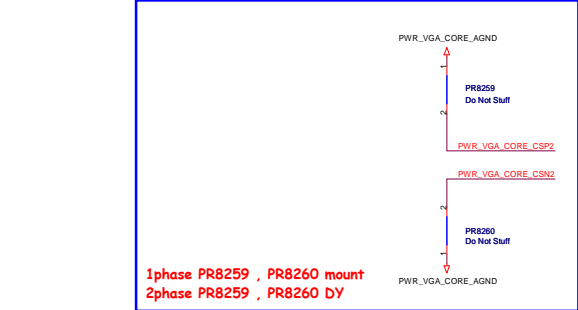
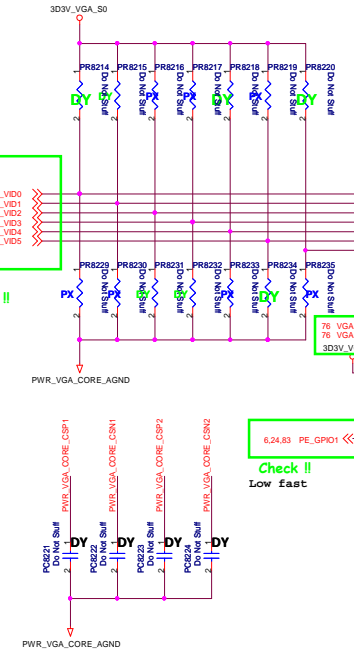
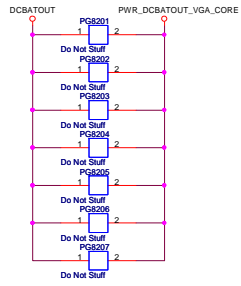








SSID = PWR.Plane.Regulator\_GFX



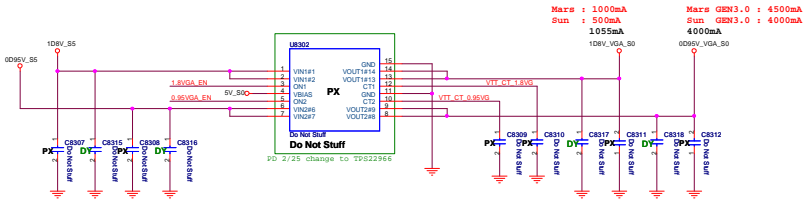
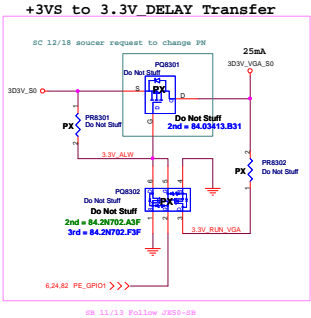
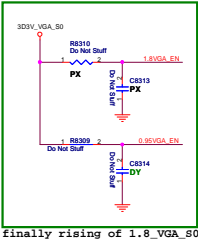
Vga\_core  
Iccmax=26A  
OCP>35A

WWW.ETECH1.RU



APL3523 for VGA\_Power

	FE_GP100	FE_GP101
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H



WWW.AITECH1.RU



WWW.AITECH1.RU

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**Wistron Corporation**  
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Title

**Switch GFX**

Size

Project Name

**KABINI**

Rev  
**SA**

Date: Friday, September 07, 2012

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WWW.AITECH1.RU

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緯創資通

**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Switch VGA**

Size

Project Name

**KABINI**

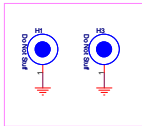
Rev  
**SA**

Date: Friday, September 07, 2012

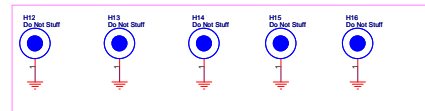
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SB 11/14 follow HW for factory issue



SB 11/20 ZZ.00pad.2T1 for change BKT size



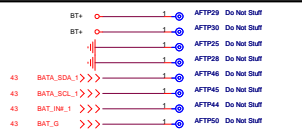
Signal	Direction	Value	Device
3D3V_S0	→	1	AFTP1 Do Not Stuff
3D3V_AUX_S0	→	1	AFTP7 Do Not Stuff
3D3V_S5	→	1	AFTP8 Do Not Stuff
5V_S5	→	1	AFTP9 Do Not Stuff
6.24 PM_PWRBNT	<<<	1	AFTP10 Do Not Stuff
24.26 APU_VRM_PWRGD	>>>	1	AFTP11 Do Not Stuff
24.36 SS_ENABLE	<<<	1	AFTP12 Do Not Stuff
4.6, 24.30, 58.65, 73.88 PLT_RST#	>>>	1	AFTP13 Do Not Stuff

Test Point放在Dimm Door打開可量測處

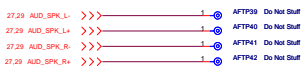
10/15 follow HT



DC IN connector



### Battery connector



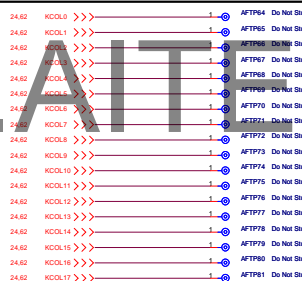
Speaker connector



HP connector



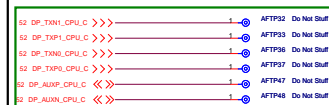
## FAN connector



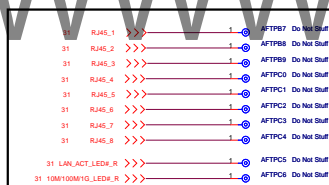
Normal KB connector



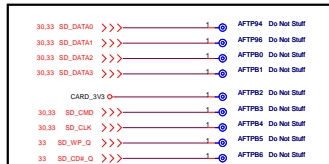
### Touch Pad connector



## EDP + MIC connector



LAN\_RJ45 connector



Card reader connector



## USBBD connector



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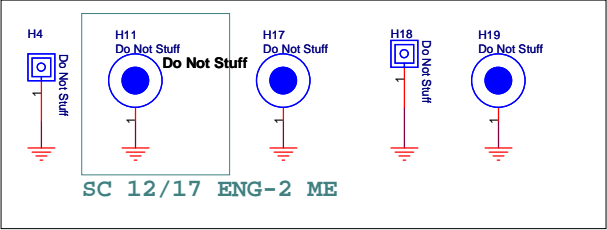
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NFC			
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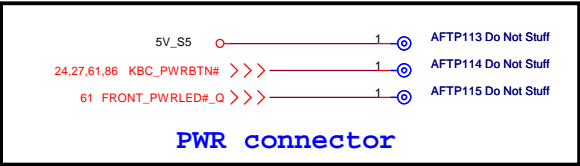




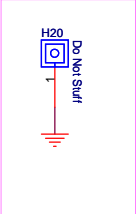
H4 & H11 & H17 & H18 & H19 for EG50



PWRBD AFTP for EG50

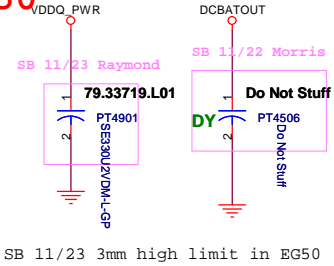
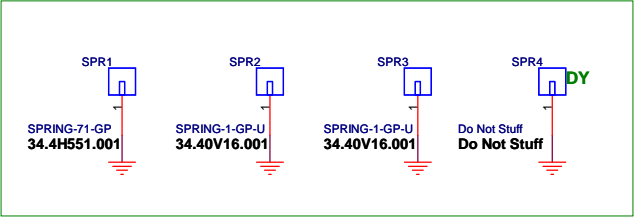


ZZ.00PAD.571



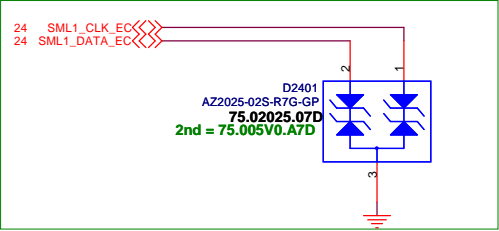
SB 11/20 location same with 14" H2

PD 1/23 EMI Jen



SB 11/23 3mm high limit in EG50

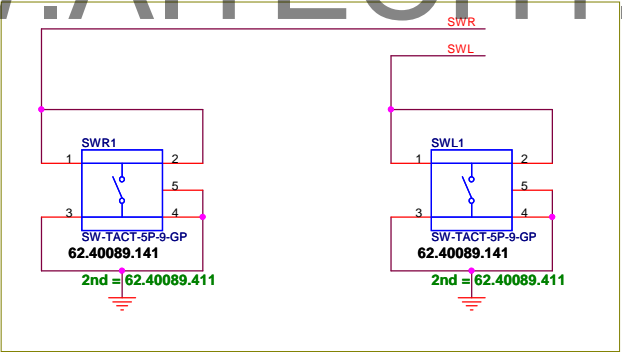
PD 01/31 Different Net name in 14" & 15" for placement



24,62,86	KCOL0	>>>
24,62,86	KCOL1	>>>
24,62,86	KCOL2	>>>
24,62,86	KCOL3	>>>
24,62,86	KCOL4	>>>
24,62,86	KCOL5	>>>
24,62,86	KCOL6	>>>
24,62,86	KCOL7	>>>
24,62,86	KCOL8	>>>
24,62,86	KCOL9	>>>
24,62,86	KCOL10	>>>
24,62,86	KCOL11	>>>
24,62,86	KCOL12	>>>
24,62,86	KCOL13	>>>
24,62,86	KCOL14	>>>
24,62,86	KCOL15	>>>
24,62,86	KCOL16	>>>
24,62,86	KCOL17	>>>
24,62,86	KROW0	>>>
24,62,86	KROW1	>>>
24,62,86	KROW2	>>>
24,62,86	KROW3	>>>
24,62,86	KROW4	>>>
24,62,86	KROW5	>>>
24,62,86	KROW6	>>>
24,62,86	KROW7	>>>

For AFTE

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PD 1/21  
SWL1 / SWR1 1st change to 62.40089.141, 2nd change to 62.40089.411 ,  
because 160kg change to 100kg.

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Title

**Smart Card socket**

Size

Project Name

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Rev

**SA**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Switchable GFX eDP**

Size

Project Name

**KABINI**

Rev

**SA**

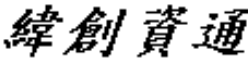
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Title			
<b>Bottom Docking</b>			
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	<b>KABINI</b>		<b>SA</b>
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**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Inter LAN WG1217LM**

Size

Project Name

**KABINI**

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**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**LAN Switch**

Size

Project Name

**KABINI**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**PCH\_XDP**

Size

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Rev

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Change History**

Size

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**SA**

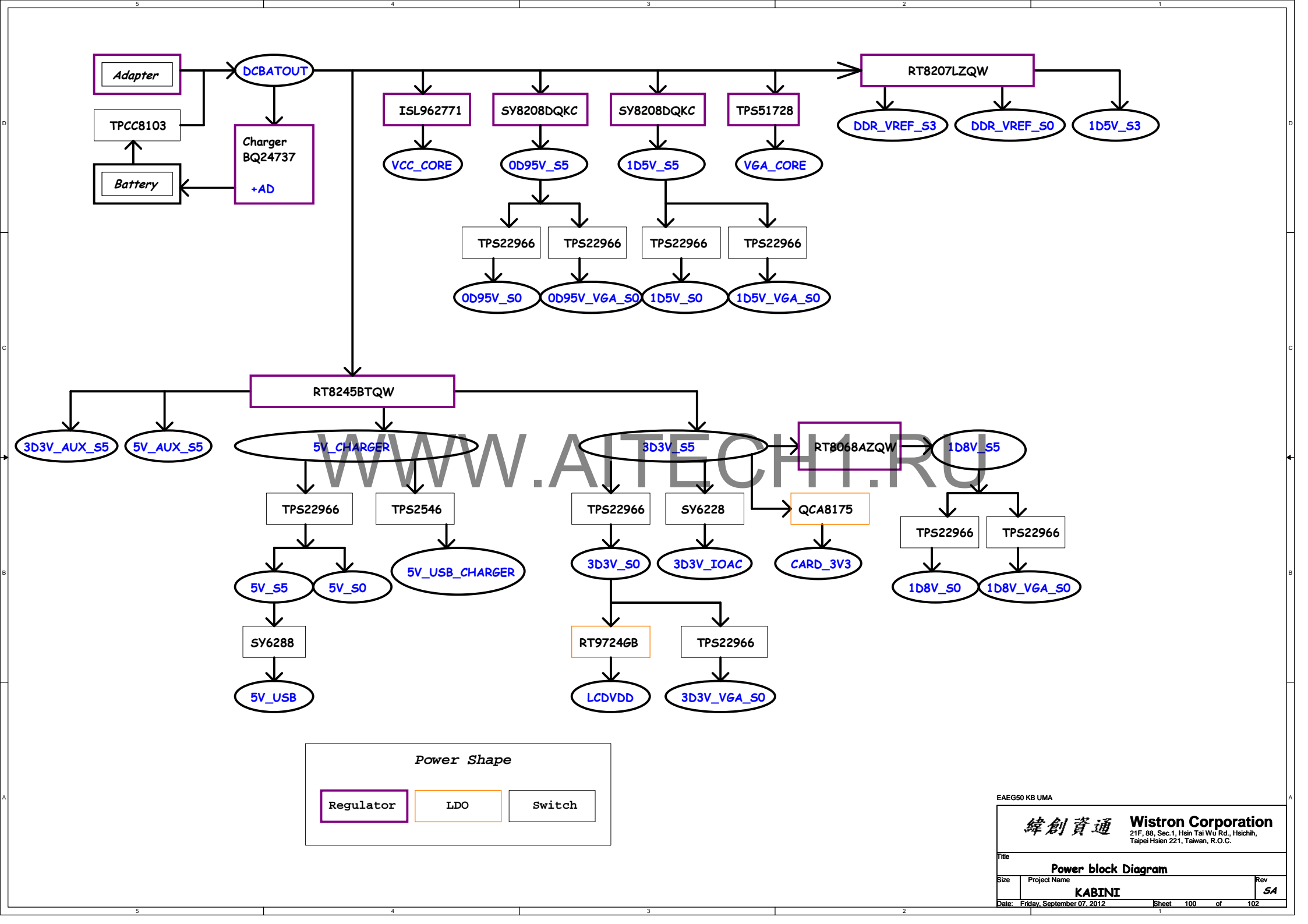
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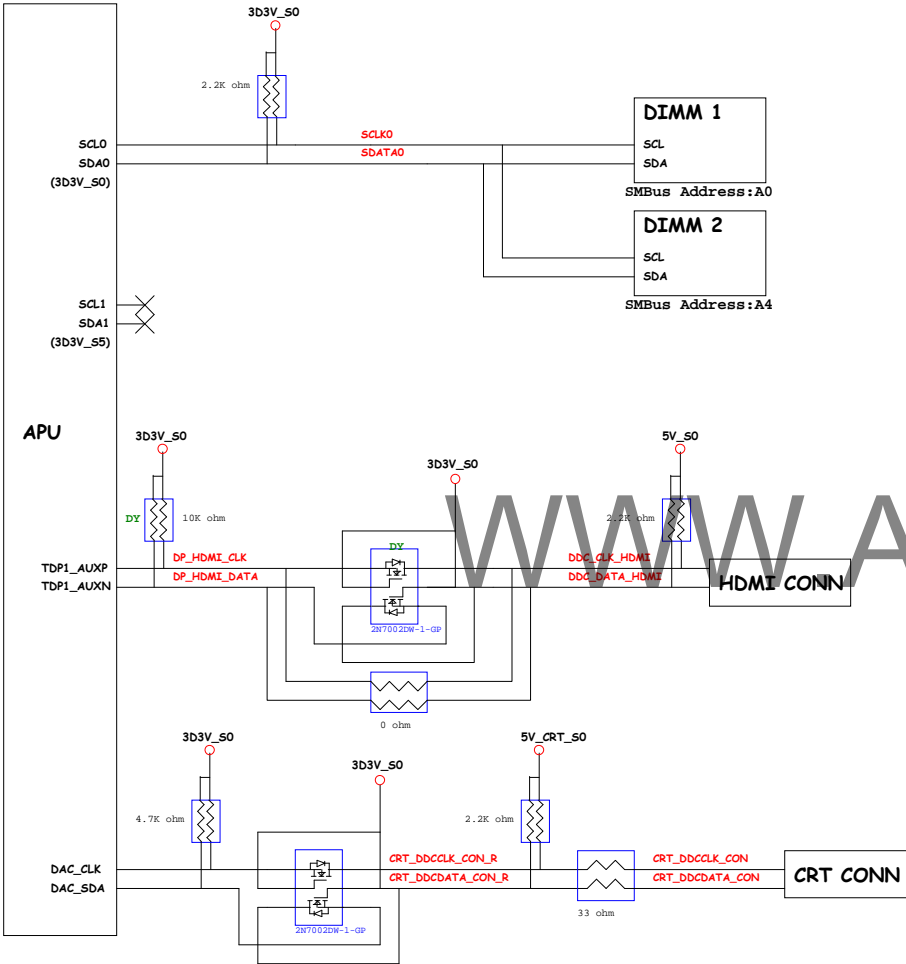
EAEG50 KB UMA

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

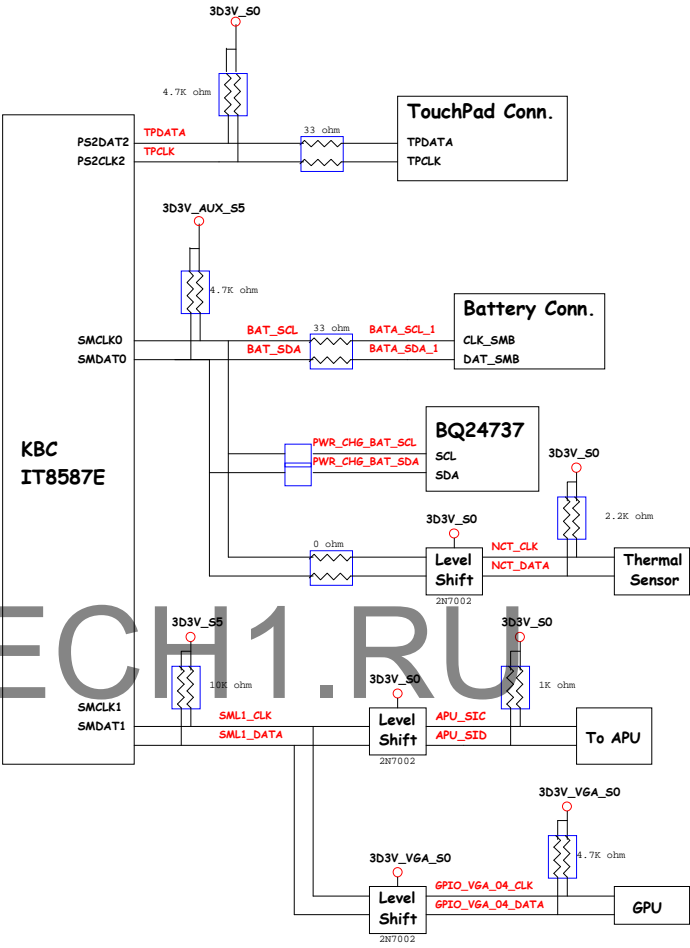
Title				
Power block Diagram				
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SMBus Block Diagram

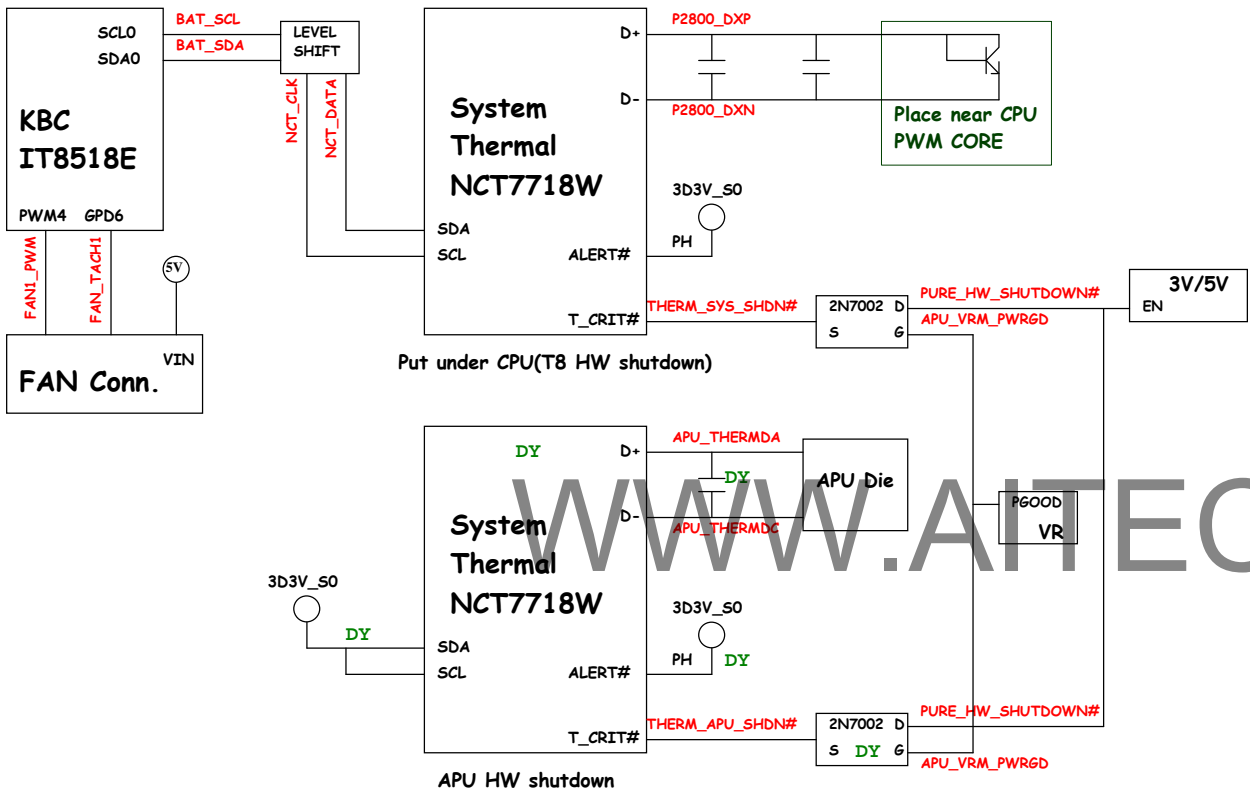


KBC SMBus Block Diagram





Thermal Block Diagram



Audio Block Diagram

